

# PLUSETECH DDR4 8GB 3200 SO-DIMM Datasheet

## PSD4B08SB32SN-08G

<b>Module Part Number</b>	PSD4B08SB32SN-08G
<b>Memory Type</b>	DDR4
<b>Module Type</b>	Unbuffered SO-DIMM
<b>Module Density</b>	8GB
<b>Data Width</b>	x64
<b>Data Rate</b>	3200 MT/s
<b>V<sub>DD</sub> Voltage</b>	1.2V
<b>Interface</b>	260-pin
<b>Number of Ranks</b>	1
<b>SDRAM Device Width</b>	x8
<b>CAS Latency</b>	CL22
<b>Operation Temperature</b>	0°C ~ +85°C
<b>RoHS</b>	Yes
<b>Standard</b>	JEDEC

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## **Features**

- JEDEC Standard
- 260-pin, small outline dual in-line memory module(SO-DIMM)
- Fast data transfer rates: PC4-3200, backward compatible PC4-3000,PC4-2666,PC4-2400, PC4-2133
- 8GB (1G x 8 x 8PCS)
- $V_{DD} = 1.2V$  (1.14-1.26V)
- Backward compatible to  $V_{DD} = 1.2V \pm 0.06V$
- $V_{DDSPD} = 2.5V$
- Nominal and dynamic on-die termination(ODT) for data, strobe, and mask signals
- Single-rank
- 16 internal banks
- Bi-Directional Differential Data Strobe
- Programmable CAS latency 15, 16, 17, 18, 19, 20, 21, 22 supported

- On board I<sup>2</sup>C with integrated serial presence-detect(SPD) EEPROM
- JEDEC standard 78ball FBGA(x8)
- Gold edge contacts
- This product in compliance with the RoHS directive
- Terminated control, command, and address bus

## **Options**

- Operation temperature
  - Commercial 0°C ~ +85°C
- Package
  - 260-pin DIMM
- Frequency/CAS latency
  - 0.625ns @ CL = 22(DDR4-3200)

**Table 1: Key Timing Parameters**

Part Number	Industrial Nomenclature	CAS Latency(CL)							
		22	21	20	19	18	17	16	15
PSD4B08SB32SN-08G	Pc4-3200	3200							
	PC4-3000		3000	3000					
	PC4-2666				2666	2666	2400	2133	2133
	PC4-2400					2400	2400	2133	2133
	PC4-2133							2133	2133

**Table 2: Addressing**

Parameter	8GB
<b>Device Configuration</b>	1Gb x 8bit x 8 pcs
<b>ROW address</b>	64K (A[14:0])
<b>Column address</b>	1K (A[9:0])
<b>Device bank group address</b>	4 (BG[1:0])
<b>Device bank address per group</b>	4 (BA[1:0])

**Table 3: DDR4-3200 Speed Bins**

Speed Bin		DDR4-3200		Unit	Note
CL - nRCD - nRP		22-22-22			
Parameter	Symbol	min	max		
Internal read command to first data	$t_{AA}$	13.75	19	ns	
ACT to internal read or write delay time	$t_{RCD}$	13.75	-	ns	
PRE command period	$t_{RP}$	13.75	-	ns	
ACT to ACT or REF command period	$t_{RC}$	45.75	-	ns	
ACT to PRE command period	$t_{RAS}$	32	$9 * t_{REFI}$	ns	

**Table 4: Operating Conditions**
**Recommended DC Operating Conditions – DDR4 (1.2V) operation**

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V <sub>DD</sub>	Supply Voltage	1.14	1.2	1.26	V	1,2,3
V <sub>DDQ</sub>	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3

**Notes:**

1. Under all conditions, V<sub>DDQ</sub> must be less than or equal to V<sub>DD</sub>.
2. V<sub>DDQ</sub> tracks with V<sub>DD</sub>. AC parameters are measured with V<sub>DD</sub> and V<sub>DDQ</sub> tied together.
3. Under these supply voltages, the device operates to this DDR4 specification.

**Table 5: DRAM Component Operating Temperature Range**

Symbol	Parameter	Rating	Units	Notes
T <sub>OPER</sub>	Normal Operating Temperature Range	0 to 85	°C	1,2

**Notes:**

1. Operating Temperature T<sub>OPER</sub> is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions.

**Table 6 : Absolute Maximum DC Ratings**

Symbol	Parameter	Rating	Units	Notes
V <sub>DD</sub>	Voltage on V <sub>DD</sub> pin relative to V <sub>SS</sub>	-0.4V~1.5V	V	1,3
V <sub>DDQ</sub>	Voltage on V <sub>DDQ</sub> pin relative to V <sub>SS</sub>	-0.4V~1.5V	V	1,3
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin relative to V <sub>SS</sub>	-0.4V~1.4V	V	1
T <sub>STG</sub>	Storage Temperature	-55 to +100	°C	1,2

**Notes:**

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. V<sub>DD</sub> and V<sub>DDQ</sub> must be within 300mV of each other at all times; and V<sub>REF</sub> must not be greater than 0.6\*V<sub>DDQ</sub>, When V<sub>DD</sub> and V<sub>DDQ</sub> are less than 500mV; V<sub>REF</sub> may be equal to or less than 300mV.

## **PCB Feature overview**

### ➤ **General**

- \* Board size: 69.6 x 30 mm ±0.15 mm
- \* Finished Board Thickness: 1.2 ±0.1 mm

\* Panel: 6 pieces PCB per panel

### \* **8-layer board**

- \* Impedance: 50/55 Ohm ±10% (Single-ended)  
83/93 Ohm ±15% (Differential)

\* **Pin count: 260 PIN**

### ➤ **PCB Material**

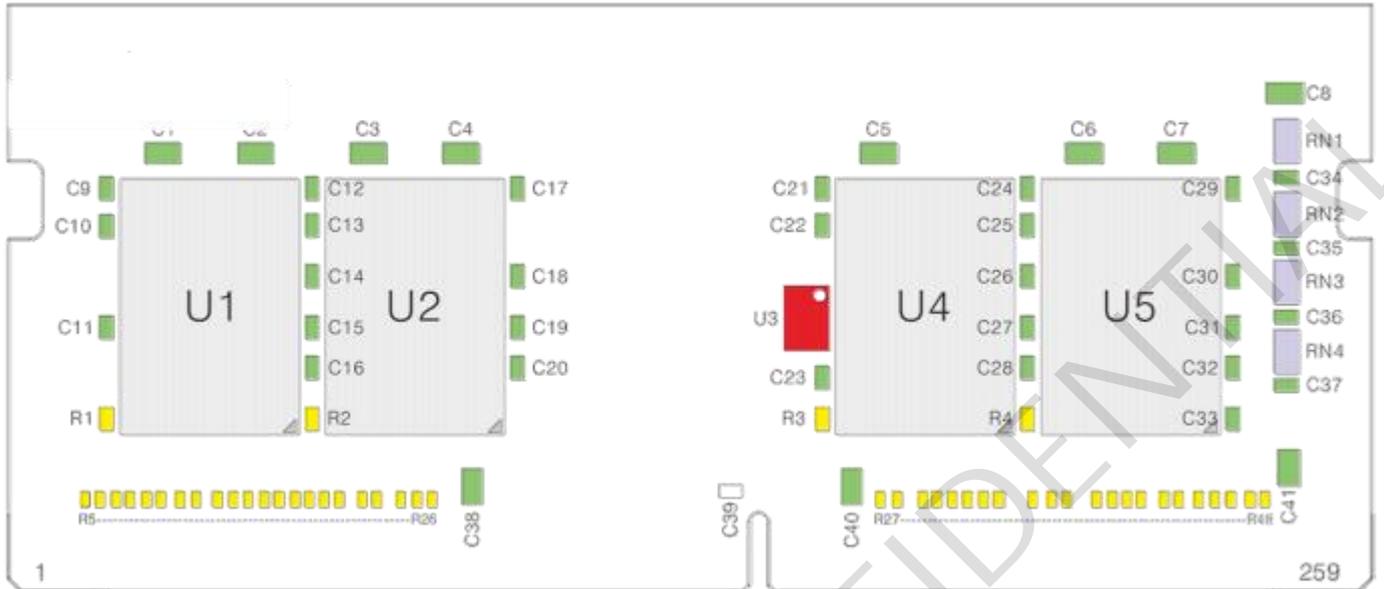
\* Glass Epoxy FR4, .UL 94V-0, BP ML

### ➤ **Plating**

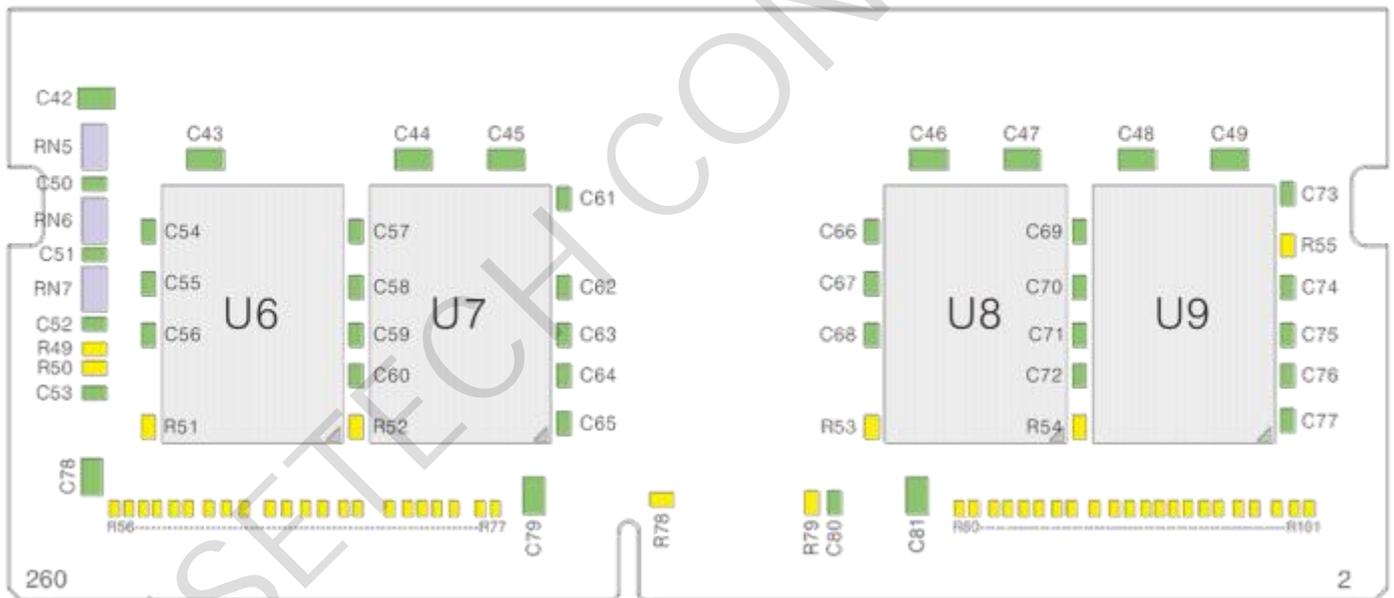
- \* Edge Connector Plating: Nickel Followed by gold
  - Nickel Plating Thickness: 100 u" min.
  - Surface treatment:
    - Gold Plating: 3u" min.
    - SMT PAD: average 2~3u".



# TOP SIDE 1-RANK WITHOUT ECC



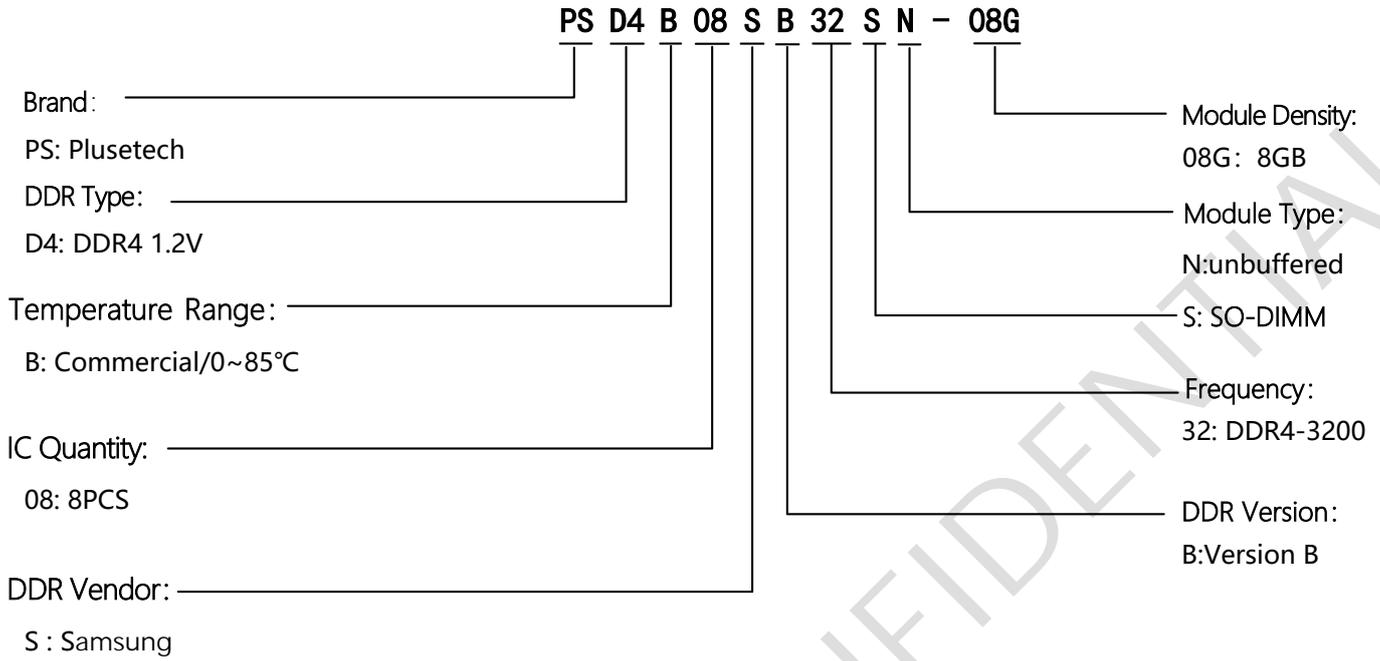
# BOTTOM SIDE 1-RANK WITHOUT ECC



**Notes:**

1. All dimensions are in millimeters (mm), MAX/MIN or typical(TYP) where noted.
2. All dimensions diagrams is for reference only.

## Part Number Decode



## Revision History

### **Rev.A0 – 12/22**

- Initial release.