eMMC 5.1 Specification

4GB, FBGA-153 Ball

Lead-Free&Halogen-Free

(RoHS Compliant)

PS04GAAJS-05S6

The PLUSETECH logo is a registered trademark of Plusetech Technology (SHENZHEN) CO., LIMITED© 2018 PLUSETECH · Printed in China · All rights reserved.

Plusetech Technology (SHENZHEN) CO., LIMITED

Add: 2402B, Block A, Tianan Digital Time Building, No. 6, Taian 4th Road, Shatou Street, Futian District, Shenzhen
Phone: 0755-86573183
Fax: 0755-86573183
Email: sales@plusetech.com
Website: http://www.plusetech.com

Revision History

Version	Revision Description	Release Date
V1.0	First release	2026.06
V1.1	- Corrected the VCCQ voltage range in the electrical characteristics and the voltage parameters for each operating mode - Added bus levels in push-pull mode, general operating conditions and bus timing parameters for all modes - Calibrated the default values of CID, CSD, Extended CSD and other registers - Improved register definitions, hardware design guide and ordering information	2026.09

Plusetech Technology (SHENZHEN) CO., LIMITED

Contents

1 Introduction 1
1.1 Product Overview 1
1.2 Product Information 1
1.3 Key Features 1
2 Package 4
2.1 Ball Array View 4
2.2 Pin Definitions 5
2.3 Package Dimensions 6
2.4 Product Structure 7
3 Basic Characteristics 8
3.1 Capacity 8
3.2 Power Consumption 8
3.3 Transfer Rate 8
3.4 Supported Operating Modes 9
4 Registers 9
4.1 CID Register 9
4.2 OCR Register 9
4.3 CSD Register 10
4.4 Extended CSD Register 11
4.5 RCA Register 18
4.6 DSR Register 18
5 eMMC Partitions 19
6 Operating Modes 20
6.1 Boot mode 20
6.2 Card identification mode 21
6.3 Data transfer mode 22
6.4 Interrupt mode 23
6.5 Inactive mode 23
7 Electrical Characteristics 24
7.1 General Operating Conditions 24
7.2 Power Supply Range 24
7.3 Bus Load 24
7.4 Bus Signal Levels 25
7.5 Power-up Timing 26
7.6 Recommended Circuit Capacitance 27
7.7 eMMC Bus Timing in Backward-Compatible and High-Speed Modes 27
7.8 eMMC Bus Timing in DDR Mode 29
7.9 eMMC Bus Timing in HS200 Mode 30
7.10 eMMC Bus Timing in HS400 Mode 31
8 Recommended Design 33
9 Soldering Process 34
10 Miscellaneous 34

Plusetech Technology (SHENZHEN) CO., LIMITED

1 Introduction

1.1 Product Overview

PS04GAAJS-05S6 is a consumer-grade eMMC storage chip launched by PLUSETECH, with a nominal capacity of 4GB in an FBGA153 package. PS04GAAJS-05S6 adopts the eMMC controller SA3636PWAAI and Samsung NAND FLASH. The design and production of PS04GAAJS-05S6 are fully localized in China. PS04GAAJS-05S6 integrates multiple core technologies, complies with the eMMC V5.1 protocol standard, and features strong performance, low power consumption and good compatibility, with customization services available. The built-in hardware ECC engine and global wear-leveling algorithm effectively improve NAND flash lifetime and data reliability; the standard JEDEC interface simplifies system development and shortens the time to market.

This specification describes the parameters of PLUSETECH eMMC products. PLUSETECH eMMC features low power consumption, compact package size and strong environmental endurance, and is widely used in consumer electronic devices and various industrial applications.

1.2 Product Information

Table 1 Product Information

Product Model	Nominal Capacity	NAND Type 1	Package Size 2	Package Type
PS04GAAJS-05S6	4GB	SLC	11.50×13.00×1.00(mm)	FBGA-153-Ball

1: Samsung SLC NAND.
2: The thickness in the dimensions is the maximum value; refer to the package dimension drawing for actual dimensions.

1.3 Key Features

■ Compliant with eMMC standard V5.1

- (Backward compatible with eMMC V4.5 to V5.0)

■ Bus Modes

- Data bus width: 1-bit (default), 4-bit and 8-bit
- Data transfer bandwidth: up to 400MB/s (HS400) @200MHz DDR mode with 8-bit bus width
- MMC I/F clock frequency: 0~200MHz
- MMC I/F boot frequency: 0~52MHz

■ Operating Voltage Range

- VCC (NAND FLASH core): 3.3V
- VCCQ (eMMC I/O supply): supports 3.3V / 1.8V dual voltage; 1.8V is used in high-speed modes (HS200/HS400)

■ Temperature

- Operating temperature: -25°C to 85°C
- Storage temperature: -40°C to 85°C

■ Moisture Sensitivity Level

- MSL-3

■ Weight

- 0.4±0.1g

■ Absolute Maximum Ratings

- VCC: -0.5V~4.1V
- VCCQ: -0.5V~4.1V

■ Supported Features

- HS400，HS200，DDR52，SDR52
- High Priority Interrupt (HPI)
- Background operations, BKOPS control
- Packed CMD, command queue
- Cache，Cache Flushing Report，Cache Barrier(Optional)
- Partitions, partition types, RPMB, RPMB bandwidth optimization
- Discard，Trim，Erase，Sanitize
- Write protection, secure write protection (optional)

- Lock/unlock
- Power-off notification (PON), Sleep/Awake
- Enhanced reliable write
- Boot feature，Boot partition
- Hardware/software reset
- Configurable drive strength
- Hardware ECC engine
- Device health report
- Field Firmware Update (FFU)
- Power-loss data protection
- Enhanced strobe mode

■ Warranty

- 3 years

Plusetech Technology (SHENZHEN) CO., LIMITED

2 Package

2.1 Ball Array View

153-Ball FBGA ball array top view:

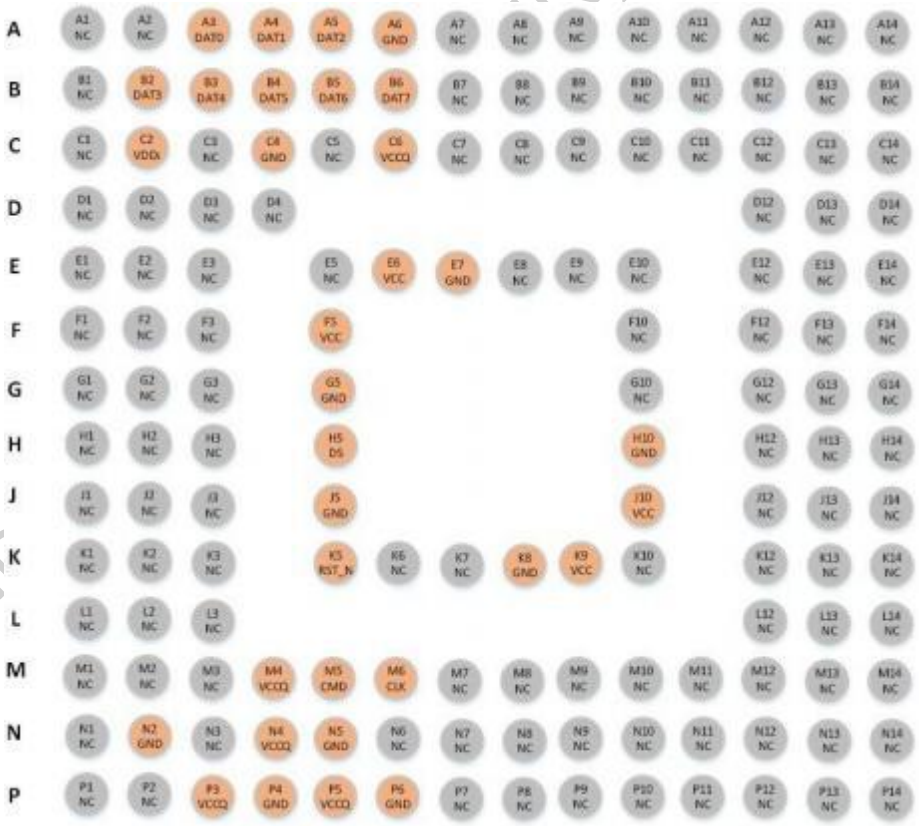


Figure 1 Top View

Table 2 Functional Pins

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A3	DAT0	H5	DS	P3	VCCQ	H10	VSS
A4	DAT1	K5	RST_N	P5	VCCQ	J5	VSS
A5	DAT2	C2	VDDi	C4	VSSQ	K8	VSS
B2	DAT3	E6	VCC	N2	VSSQ		
B3	DAT4	F5	VCC	N5	VSSQ		
B4	DAT5	J10	VCC	P4	VSSQ		
B5	DAT6	K9	VCC	P6	VSSQ		
B6	DAT7	C6	VCCQ	A6	VSS		
M6	CLK	M4	VCCQ	E7	VSS		
M5	CMD	N4	VCCQ	G5	VSS		

See 2.2 Pin Definitions for functional pin descriptions.
NC: internally not connected; leave unconnected.

2.2 Pin Definitions

Table 3 Pin Definitions

Signal	Ball No.	Type	Description
CLK	M6	I	eMMC clock input signal, used as the sampling signal for command and data signals on each clock cycle.
CMD	M5	I/O	eMMC command (response) signal, bidirectional; the host sends commands to the eMMC and the eMMC sends responses to the host. The command signal has two operating modes: open-drain (initialization), a 4.7K pull-up resistor to VCCQ is recommended; it can be configured as push-pull mode after initialization.
DATA(DAT0-DAT7)	A3，A4，A5，B2，B3，B4，B5，B6	IO	8-bit data transfer signals, bidirectional; during initialization the DAT0 line is open-drain output, a 10K pull-up resistor to VCCQ is recommended; it is set to push-pull output after initialization.
RST_N	K5	I	eMMC power-on hardware reset input (disabled by default).
DS	H5	O	eMMC DS output signal, enabled after being configured in HS400 mode; used for data synchronization with the Host, same frequency as CLK.
VCCQ	M4，N4，P3，P5	P	Power supply for the MMC interface and controller, supports two supply voltages: high voltage (low speed): 3.3V; low voltage (high speed): 1.8V.
VCC	E6，F5，J10，K9	P	NAND FLASH core power supply: 3.3V.
VDDi	C2	P/O	MMC controller core power, provided by the internal LDO; connect an external 0.1uF~2.2uF capacitor to ground.
VSSQ，VSS	A6，E7，G5，H10，J5，K8，C4，N2，N5，P4，P6	G	Ground signals.

I: Input

O: Output

I/O: Bidirectional

P: Power

G: Ground

P/O: Power output, no external supply required

2.3 Package Dimensions

153-Ball FBGA detailed dimensions:

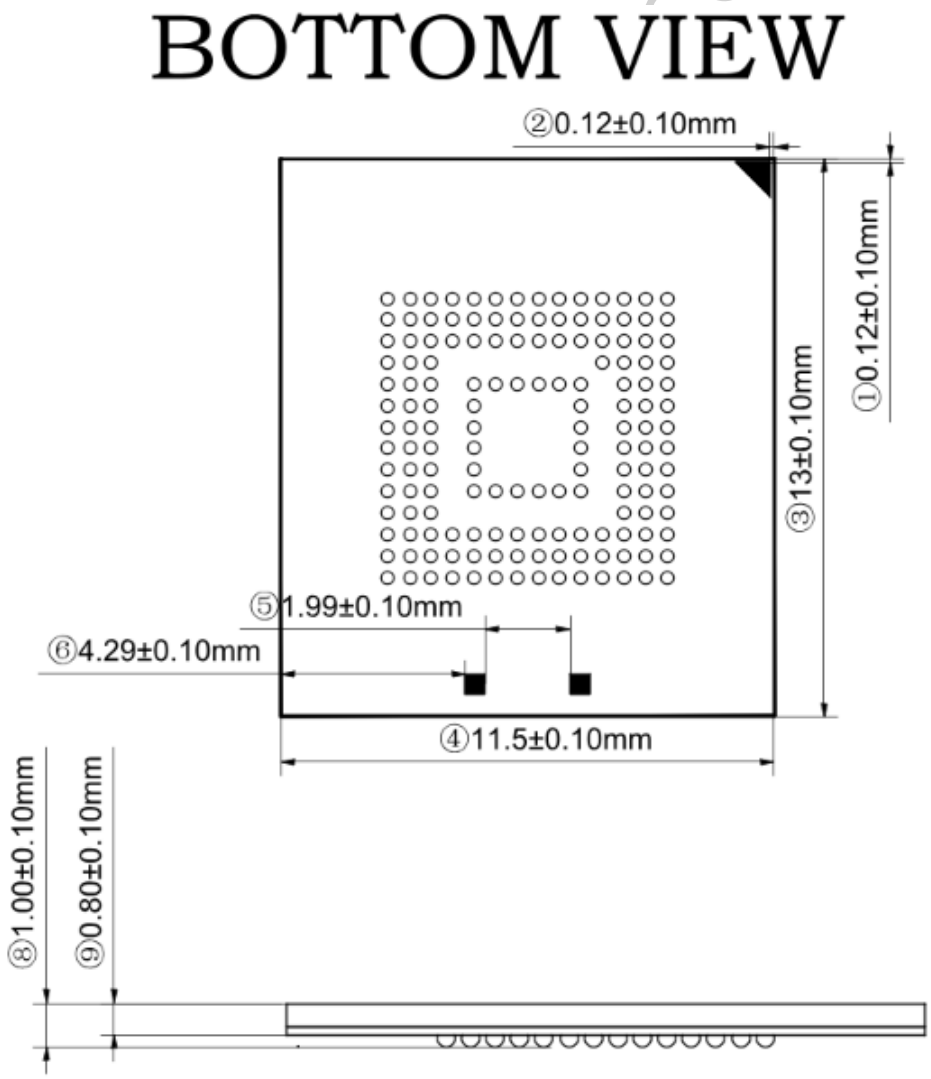


Figure 2 Package Dimensions

Note: The solder balls of the product are lead-free SAC305.

2.4 Product Structure

The eMMC internally consists of an MMC controller and NAND FLASH. The MMC controller connects to the NAND FLASH IO through the NAND IO interface and is responsible for NAND FLASH management; externally it provides the eMMC IO interface, mainly handling interface protocol parsing. An internal LDO converts the VCCQ supply into the power source for the MMC controller core logic.

From the system perspective, the eMMC device communicates with the host controller through the eMMC bus interface, which covers clock, command, data and control signals. The internal power domains of the device are divided into three parts: flash core power (VCC), I/O interface power (VCCQ), and controller core power (VDDi, generated by the internal LDO).

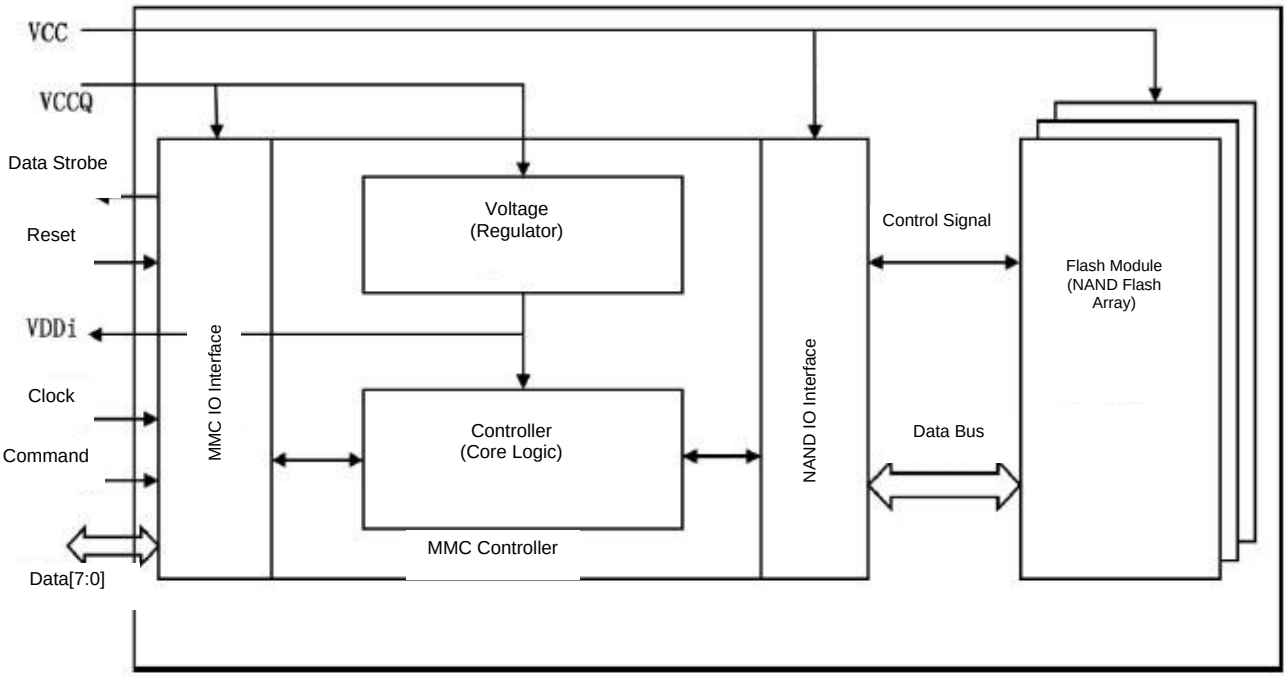


Figure 3 eMMC Block Diagram

3 Basic Characteristics

3.1 Capacity

Table 4 Capacity

Model	User Area Capacity	EXT_CSD Register Sector Count
PS04GAAJS-05S6	3830MB	0x0077B000

3.2 Power Consumption

Read/Write power consumption:

Table 5 Read/Write Power Consumption

Product Model	Transfer Mode	Read (mA)	Write (mA)
PS04GAAJS-05S6	HS400	47	44

Test conditions:

At room temperature, 8-bit bus width, HS400 mode, 512KB data block, no file system overhead, tested on the internal test board; VCC=3.3V, VCCQ=1.8V.

Supply idle power consumption:

Table 6 Idle Power Consumption

Product Model	Transfer Mode	Standby (mA)	Sleep (mA)
PS04GAAJS-05S6	/	0.033	0

Test conditions:

At room temperature, powered by VCC=3.3V, VCCQ=1.8V.

3.3 Transfer Rate

Table 7 Transfer Rate

Product Model	Test Condition	Performance	
		Sequential Write (MB/s)	Sequential Read (MB/s)
PS04GAAJS-05S6	CrystalDiskMark(1GB)	Up to 240	Up to 240

Test conditions:

8-bit bus width, HS400 mode, 512KB data transfer, no file system overhead, tested on the internal test board.

Note: The above are measured values of finished products of this model; the maximum interface rate of the controller can reach 400MB/s. Actual performance varies with capacity and Flash media.

3.4 Supported Operating Modes

Table 8 Operating Modes

Operating Mode	Clock Frequency	Power Supply	**Bus Width (bit)**
HS400 Mode	0-200MHz DDR	VCC=3.3V， VCCQ=1.8V	8
HS200 Mode	0-200MHz SDR	VCC=3.3V， VCCQ=1.8V	4、8
HS Mode	0-52MHz DDR	VCC=3.3V， VCCQ=3.3V/1.8V	4、8
	0-52MHz SDR	VCC=3.3V， VCCQ=3.3V/1.8V	1、4、8
Compatible Mode	0-26MHz SDR	VCC=3.3V， VCCQ=3.3V/1.8V	1、4、8

Note: High-speed modes (HS200/HS400) only support 1.8V VCCQ supply; compatible mode and HS mode support 3.3V/1.8V dual voltage switching.

4 Registers

4.1 CID Register

The CID register, also called the Device Identification register, is a 128-bit register. It contains the device identification information required during the device identification phase; each eMMC has a unique identification code (CID).

The following table defines the structure of the eMMC Device Identification register:

Table 9 CID Register Structure Definition

CID Bits	Register Name	Description	Width	Value
[127:120]	MID	Manufacturer ID	8	0x38
[119:114]	-	Reserved	6	0
[113:112]	CBX	Medium Type	2	0x1
[111:104]	OID	User ID	8	0x05
[103:56]	PNM	Product Name	48	PluseT
[55:48]	PRV	Product Revision	8	0xFF
[47:16]	PSN	Product Serial Number	32	-
[15:8]	MDT	Manufacturing Date	8	0x93
[7:1]	CRC	CRC Code	7	-
[0]	-	Reserved	1	0x1

Customers with special requirements may contact the manufacturer to customize the CID register contents.

4.2 OCR Register

The OCR register, also called the Operating Conditions register, is a 32-bit register containing the device voltage and access mode information. In addition, this register includes a status bit [31]; this bit is set when the device power-up process has completed.

The following table shows the structure of the eMMC Operating Conditions register:

Table 10 OCR Register

OCR Bits	VCCQ Voltage Range	Description	Width	Value
[6:0]	-	Reserved	7	000 0000b
[7]	1.7V~1.95V	Low Voltage Mode	1	1b
[14:8]	2.0V~2.6V	Mid Voltage Mode	7	000 0000b
[23:15]	2.7V~3.6V	High Voltage Mode	9	1 1111 1111b
[28:24]	-	Reserved	5	0 0000b
[30:29]	Access Mode	Access Mode	2	10b(sector mode)
[31]	status bit	Device Status Bit	1	Busy (0)/ready (1)

4.3 CSD Register

The CSD register provides information on how to access the eMMC contents; it is a 128-bit register. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register is available, etc. The programmable part of the register (see access types below) can be changed by CMD27.

The access types are divided into 8 categories:

R: Read-only

W: One-time programmable, not readable

R/W: One-time programmable, readable

W/E: Multiple writable, not readable; value retained after power-off, H/W reset or CMD0 reset

R/W/E: Multiple writable and readable; value retained after power-off, H/W reset or CMD0 reset

R/W/C_P: Writable and readable; the value is cleared after power-off or H/W reset

R/W/E_P: Multiple writable and readable; the value is reset after power-off, H/W reset or CMD0

W/E/_P: Multiple writable, not readable; the value is reset after power-off, H/W reset or CMD0

Table 11 CSD Register

CSD Bits	Field	Description	Access Type	Width	Value
[127:126]	CSD_STRUCTURE	CSD Structure	R	2	11b
[125:122]	SPEC_VERS	System Specification Version	R	4	0100b
[121:120]	-	Reserved	R	2	00b
[119:112]	TAAC	Data Read Access Time	R	8	01111111b
[111:104]	NSAC	Data read access time in clock cycles	R	8	00000001b
[103:96]	TRAN_SPEED	Max. Bus Clock Frequency	R	8	00101010b
[95:84]	CCC	Device Command Classes	R	12	100111110101b
[83:80]	READ_BL_LEN	Max. Read Data Block Length	R	4	1001b
[79:79]	READ_BL_PARTIAL	Partial Blocks for Read Allowed	R	1	0b
[78:78]	WRITE_BLK_MISALIGN	Write Block Misalignment	R	1	0b
[77:77]	READ_BLK_MISALIGN	Read Block Misalignment	R	1	0b

CSD Bits	Field	Description	Access Type	Width	Value
[76:76]	DSR_IMP	DSR Supplement	R	1	0b
[75:74]	-	Reserved	R	2	00b
[73:62]	C_SIZE	Device Capacity	R	12	111111111111b
[61:59]	VDD_R_CURR_MIN	Max. Read Current @VDD min	R	3	110b
[58:56]	VDD_R_CURR_MAX	Max. Read Current @VDD max	R	3	110b
[55:53]	VDD_W_CURR_MIN	Max. Write Current @VDD min	R	3	110b
[52:50]	VDD_W_CURR_MAX	Max. Write Current @VDD max	R	3	110b
[49:47]	C_SIZE_MULT	Device Capacity Multiplier	R	3	111b
[46:42]	ERASE_GRP_SIZE	Erase Group Size	R	5	11111b
[41:37]	ERASE_GRP_MULT	Erase Group Size Multiplier	R	5	11111b
[36:32]	WP_GRP_SIZE	Write Protection Group Size	R	5	01111b
[31:31]	WP_GRP_MULT	Write Protection Group Enable	R	1	1b
[30:29]	ECC DEFAULT_ECC	ECC DEFAULT_ECC	R	2	00b
[28:26]	R2W_FACTOR	Write Speed Factor	R	3	001b
[25:22]	WRITE_BL_LEN	Max. Write Data Block Length	R	4	1001b
[21:21]	WRITE_BL_PARTIAL	Partial Blocks for Write Allowed	R	1	0b
[20:17]	-		R	4	0000b
[16:16]	CONTENT_PROT_APP	Content Protection Application	R	1	0b
[15:15]	FILE_FORMAT_GRP	File Format Group	R/W	1	0b
[14:14]	COPY	Copy Flag	R/W	1	0b
[13:13]	PERM_WRITE_PROTECT	Permanent Write Protection	R/W	1	0b
[12:12]	TMP_WRITE_PROTECT	Temporary Write Protection	R/W/E	1	0b
[11:10]	FILE_FORMAT	File Format	R/W	2	00b
[9:8]	ECC	ECC	R/W/E	2	00b
[7:1]	CRC	CRC	R/W/E	7	1110011b
[0]	-		-	1	1b

4.4 Extended CSD Register

The Extended CSD register defines eMMC attributes and selected modes; it is a 512-byte register. The upper 320 bytes are the attributes field, which defines the eMMC capacity and cannot be modified by the host. The lower 192 bytes are the mode field, which defines the configuration currently used by the eMMC. The host can modify these configurations via the SWITCH command (CMD6).

The access types are divided into 8 categories:

R: Read-only

W: One-time programmable, not readable

R/W: One-time programmable, readable

W/E: Multiple writable, not readable; value retained after power-off, H/W reset or CMD0 reset

R/W/E: Multiple writable and readable; value retained after power-off, H/W reset or CMD0 reset

R/W/C_P: Writable and readable; the value is cleared after power-off or H/W reset

R/W/E_P: Multiple writable and readable; the value is reset after power-off, H/W reset or CMD0

W/E/_P: Multiple writable, not readable; the value is reset after power-off, H/W reset or CMD0

Table 12 Extended CSD Register

CSD Bits	Field	Description	Access Type	Size (Bytes)	Value
[511:506]	-	Reserved	TBD	6	-
[505]	EXT_SECURITY_ERR	Extended Security Command Error	R	1	0x00
[504]	S_CMD_SET	Supported Command Sets	R	1	0x01
[503]	HPI_FEATURES	HPI Feature	R	1	0x03
[502]	BKOPS_SUPPORT	Background Operation Support	R	1	0x01
[501]	MAX_PACKED_READS	Max. Packed Read Commands	R	1	0x3F
[500]	MAX_PACKED_WRITES	Max. Packed Write Commands	R	1	0x3F
[499]	DATA_TAG_SUPPORT	Data Tag Support	R	1	0x01
[498]	TAG_UNIT_SIZE	Tag Unit Size	R	1	0x01
[497]	TAG_RES_SIZE	Tag Resource Size	R	1	0x00
[496]	CONTEXT_CAPABILITIES	Context Management Capability	R	1	0x05
[495]	LARGE_UNIT_SIZE_M1	Large Unit Size	R	1	0x00
[494]	EXT_SUPPORT	Extended Partition Attribute Support	R	1	0x03
[493]	SUPPORTED_MODES	Supported Modes	R	1	0x01
[492]	FFU_FEATURES	FFU Function	R	1	0x01
[491]	OPERATION_CODE_TIME OUT	Operation Code Timeout	R	1	0x17
[490:487]	FFU_ARG	FFU Operation Code	R	4	0x00
[486]	BARRIER_SUPPORT	Masking Support	R	1	0x00
[485:309]	-	Reserved	TBD	-	-
[308]	CMDQ_SUPPORT	Command Queue Support	R	1	0x01
[307]	CMDQ_DEPTH	Command Queue Depth	R	1	0x07
[306]	-	Reserved	TBD	1	-
[305:302]	NUMBER_OF_FW_SECTORS _CORRECTLY_PROGR AMMED	Correctly Programmed Sector Count	R	4	0x00
[301:270]	VENDOR_PROPRIETARY_ HEALTH_REPORT	Vendor Health Report	R	32	0x00
[269]	DEVICE_LIFE_TIME_EST _TYP_B	Lifetime	R	1	0x01
[268]	DEVICE_LIFE_TIME_EST _TYP_A	Lifetime	R	1	0x01
[267]	PRE_EOL_INFO	Pre-EOL Information	R	1	0x01
[266]	OPTIMAL_READ_SIZE	Optimal Read Size	R	1	0x08
[265]	OPTIMAL_WRITE_SIZE	Optimal Write Size	R	1	0x08
[264]	OPTIMAL_TRIM_UNIT_SIZE	TRIM Optimal Unit Size	R	1	0x08
[263:262]	DEVICE_VERSION	Device Version	R	2	0x0000
[261:254]	FIRMWARE_VERSION	Firmware Version	R	8	0xF0616
[253]	PWR_CL_DDR_200_360	1	R	1	0x00

CSD Bits	Field	Description	Access Type	Size (Bytes)	Value
[252:249]	CACHE_SIZE	Cache Size	R	4	0x100
[248]	GENERIC_CMD6_TIME	Generic CMD6 Timeout	R	1	0x32
[247]	POWER_OFF_LONG_TIME	Power-off Notification (long) Timeout	R	1	0x3C
[246]	BKOPS_STATUS	Background Operation Status	R	1	0x00
[245:242]	CORRECTLY_PRG_SECTORS_NUM	Correctly Programmed Sectors	R	4	0x00
[241]	INI_TIMEOUT_AP	First Init Time After Partitioning	R	1	0x1E
[240]	CACHE_FLUSH_POLICY	Cache Flushing Policy	R	1	0x00
[239]	PWR_CL_DDR_52_360	52MHz DDR 3.6V Power Level	R	1	0x00
[238]	PWR_CL_DDR_52_195	52MHz DDR 1.95V Power Level	R	1	0x00
[237]	PWR_CL_200_195	200MHz 1.95V Power Class	R	1	0x00
[236]	PWR_CL_200_130	200MHz 1.3V Power Class	R	1	0x00
[235]	MIN_PERF_DDR_W_8_52	8-bit 52MHz DDR Mode Min. Write Performance	R	1	0x00
[234]	MIN_PERF_DDR_R_8_52	8-bit 52MHz DDR Mode Min. Read Performance	R	1	0x00
[233]	-	Reserved	TBD	1	-
[232]	TRIM_MULT	MULT TRIM	R	1	0x02
[231]	SEC_FEATURE_SUPPORT	Multi-Sector Support	R	1	0x55
[230]	SEC_ERASE_MULT	Multi-Sector Erase	R	1	0x1B
[229]	SEC_TRIM_MULT	Multi-Sector TRIM	R	1	0x11
[228]	BOOT_INFO	Boot Information	R	1	0x07
[227]	-	Reserved	TBD	1	-
[226]	BOOT_SIZE_MULT	Boot Partition Size	R	1	0x20
[225]	ACC_SIZE	Access Length	R	1	0x06
[224]	HC_ERASE_GRP_SIZE	High-Capacity Erase Unit Size	R	1	0x01
[223]	ERASE_TIMEOUT_MULT	MULT Erase Timeout	R	1	0x01
[222]	REL_WR_SEC_C	Reliable Write Sector Count	R	1	0x01
[221]	HC_WP_GRP_SIZE	High-Capacity Write Protection Group Size	R	1	0x10
[220]	S_C_VCC	Sleep Current VCC	R	1	0x07
[219]	S_C_VCCQ	Sleep Current VCCQ	R	1	0x07
[218]	PRODUCTION_STATE_AWARENESS_TIMEOUT	Production State Awareness Timeout	R	1	0x17
[217]	S_A_TIMEOUT	1	R	1	0x17
[216]	SLEEP_NOTIFICATION_TIME	Sleep Notification Time	R	1	0x11
[215:212]	SEC_COUNT	Total Sector Count	R	4	0x0077B000
[211]	SECURE_WP_INFO	Secure Write Protection Info	R	1	0x00
[210]	MIN_PERF_W_8_52	8-bit 52MHz Min. Write Performance	R	1	0x00
[209]	MIN_PERF_R_8_52	8-bit 52MHz Min. Read Performance	R	1	0x00

CSD Bits	Field	Description	Access Type	Size (Bytes)	Value
[208]	MIN_PERF_W_8_26_4_52	8bit 26MHz/4bit 52MHz Min. Write Performance	R	1	0x00
[207]	MIN_PERF_R_8_26_4_52	8bit 26MHz/4bit 52MHz Min. Read Performance	R	1	0x00
[206]	MIN_PERF_W_4_26	4-bit 26MHz Min. Write Performance	R	1	0x00
[205]	MIN_PERF_R_4_26	4-bit 26MHz Min. Read Performance	R	1	0x00
[204]	-	Reserved	TBD	1	-
[203]	PWR_CL_26_360	/	R	1	0x00
[202]	PWR_CL_52_360	/	R	1	0x00
[201]	PWR_CL_26_ 195	/	R	1	0x00
[200]	PWR_CL_52_ 195	/	R	1	0x00
[199]	PARTITION_SWITCH_TIME	Partition Switch Timing	R	1	0x05
[198]	OUT_OF_INTERRUPT_TIME	Out-of-interrupt busy timing	R	1	0x19
[197]	DRIVER_STRENGTH	I/O Driver Strength	R	1	0x1F
[196]	DEVICE_TYPE	Device Type	R	1	0x57
[195]	-	Reserved	TBD	1	-
[194]	CSD_STRUCTURE	CSD Structure Version	R	1	0x02
[193]	-	Reserved	TBD	1	-
[192]	EXT_CSD_REV	Extended CSD Version	R	1	0x08
[191]	CMD_SET	Command Set	R/W/E_P	1	0x00
[190]	-	Reserved	TBD	1	-
[189]	CMD_SET_REV	Command Set Version	R	1	0x00
[188]	-	Reserved	TBD	1	-
[187]	POWER_CLASS	Power Class	R/W/E_P	1	0x00
[186]	-	Reserved	TBD	1	-
[185]	HS_TIMING	High-Speed Interface Timing	R/W/E_P	1	0x00
[184]	STROBE_SUPPORT	STROBE Support	R	1	0x01
[183]	BUS_WIDTH	Bus Width Mode	W/E_P	1	0x00
[182]	-	Reserved	TBD	1	-
[181]	ERASE_MEM_CONT	Erased Memory Content	R	1	0x00
[180]	-	Reserved	TBD	1	-
[179]	PARTITION_CONFIG	Partition Configuration	R/W/E&R/W/E_P	1	0x00
[178]	BOOT_CONFIG_PROT	Boot Area Configuration Protection	R/W&R/W/C_P	1	0x00
[177]	BOOT_BUS_CONDITIONS	Boot Bus Conditions	R/W/E	1	0x00
[176]	-	Reserved	TBD	1	-
[175]	ERASE_GROUP_DEF	Erase Group Definition	R/W/E	1	0x00
[174]	BOOT_WP_STATUS	Boot Write Protection Status Register	R	1	0x00
[173]	BOOT_WP	Boot Area Write Protection Register	R/W&R/W/C_P	1	0x00
[172]	-	Reserved	TBD	1	-

CSD Bits	Field	Description	Access Type	Size (Bytes)	Value
[171]	USER_WP	User Area Write Protection Register	R/W，R/W/C_P& R/W/E_P	1	0x00
[170]	-	Reserved	TBD	1	-
[169]	FW_CONFIG	FW Configuration	R/W	1	0x00
[168]	RPMB_SIZE_MULT	RPMB Size	R	1	0x20
[167]	WR_REL_SET	Write Reliability Setting Register	R/W	1	0x00
[166]	WR_REL_PARAM	Write Reliability Parameter Register	R	1	0x15
[165]	SANITIZE_START	Start Sanitize Operation	W/E_P	1	0x00
[164]	BKOPS_START	Start Background Operation	W/E_P	1	0x00
[163]	BKOPS_EN	Enable Background Operations	R/W&R/W/E	1	0x00
[162]	RST_n_FUNCTION	Hardware Reset Function	R/W	1	0x00
[161]	HPI_MGMT	HPI Management	R/W/E_P	1	0x00
[160]	PARTITIONING_SUPPORT	Partition Support	R	1	0x07
[159:157]	MAX_ENH_SIZE_MULT	Max. Enhanced Area Size	R	3	0x0001DF
[156]	PARTITIONS_ATTRIBUTE	Partition Attribute	R/W	1	0x00
[155]	PARTITION_SETTING_COMPLETED	Partition Setting	R/W	1	0x00
[154:143]	GP_SIZE_MULT	General Partition Size	R/W	12	0x00
[142:140]	ENH_SIZE_MULT	Enhanced User Data Area Size	R/W	3	0x00
[139:136]	ENH_START_ADDR	Enhanced User Data Start Address	R/W	4	0x00
[135]	-	Reserved	TBD	1	-
[134]	SEC_BAD_BLK_MGMNT	Bad Block Management Mode	R/W	1	0x00
[133]	PRODUCTION_STATE_AWARENES	Production State Awareness	R/W/E	1	0x00
[132]	TCASE_SUPPORT	Case Temperature Controlled	W/E_P	1	0x00
[131]	PERIODIC_WAKEUP	Periodic Wake-up	R/W/E	1	0x00
[130]	PROGRAM_CID_CSD_DDR_SUPPORT	CID/CSD Programming in DDR Mode Support	R	1	0x01
[129:128]	-	Reserved	TBD	2	-
[127:64]	VENDOR_SPECIFIC_FIELD	Vendor Specific Field	-	64	0x00
[63]	NATIVE_SECTOR_SIZE	Native Sector Size	R	1	0x00
[62]	USE_NATIVE_SECTOR	Native User Sectors	R/W	1	0x00
[61]	DATA_SECTOR_SIZE	Sector Size	R	1	0x00
[60]	INI_TIMEOUT_EMU	Initialization Timeout	R	1	0x00
[59]	CLASS_6_CTRL	Class 6 Command Control	R/W/E_P	1	0x00
[58]	DYNCAP_NEEDED	Released Addressed Groups	R	1	0x00
[57:56]	EXCEPTION_EVENTS_CTRL	Exception Event Control	R/W/E_P	2	0x00
[55:54]	EXCEPTION_EVENTS_STATUS	Exception Event Status	R	2	0x00
[53:52]	EXT_PARTITIONS_ATTRI	Extended Partition Attribute	R/W	2	0x00

CSD Bits	Field	Description	Access Type	Size (Bytes)	Value
	BUTE				
[51:37]	CONTEXT_CONF	Context Configuration	R/W/E_P	15	0x00
[36]	PACKED_COMMAND_STAUS	Packed Command Status	R	1	0x00
[35]	PACKED_FAILURE_INDEX	Packed Command Failure Index	R	1	0x00
[34]	POWER_OFF_NOTIFICATION	Power-off Notification	R/W/E_P	1	0x00
[33]	CACHE_CTRL	CACHE On/Off Control	R/W/E_P	1	0x00
[32]	FLUSH_CACHE	FLUSH_CACHE	W/E_P	1	0x00
[31]	BARRIER_CTRL	BARRIER_CTRL	R/W	1	0x00
[30]	MODE_CONFIG	Mode Control	R/W/E_P	1	0x00
[29]	MODE_OPERATION_CODES	Mode Operation Code	W/E_P	1	0x00
[28:27]	-	Reserved	TBD	2	-
[26]	FFU_STATUS	FFU Status	R	1	0x00
[25:22]	PRE_LOADING_DATA_SIZE	Pre-loading Data Size	R/W/E_P	4	0x00
[21:18]	MAX_PRE_LOADING_DATA_SIZE	Max. Pre-loading Data Size	R	4	0x0077C000
[17]	PRODUCT_STATE_AWARENESS_ENABLEMENT	Production State Awareness Enable	R/W/E&R	1	0x03
[16]	SECURE_REMOVAL_TYPE	Secure Erase Type	R/W&R	1	0x09
[15]	CMDQ_MODE_EN	Multi-Command Mode Enable	R/W/E_P	1	0x00
[14:0]	-	Reserved	TBD	15	-

4.4.1 EXT_CSD_REV [192]

This register describes the protocol versions supported by the device.

Table 13 Protocol Version

Protocol Version	Value	Default Value
Reserved	255–9	0x08
Revision 1.8(for MMC V5.1)	8	
Revision 1.7(for MMC V5.0)	7	
Revision 1.6(for MMC V4.5，V4.51)	6	
Revision 1.5(for MMC V4.41)	5	
Revision 1.4(Obsolete)	4	
Revision 1.3(for MMC V4.3)	3	
Revision 1.2(for MMC V4.2)	2	
Revision 1.1(for MMC V4.1)	1	
Revision 1.0(for MMC V4.0)	0	

4.4.2 HS_TIMING [185]

Table 14 Timing Interface Speed and Drive Strength

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Drive Strength Setting				Timing Interface Speed			

This register is used by the host to select the timing interface speed and driver strength. This byte consists of two fields:

bit[3:0]: Timing interface speed, power-on default 0.

bit[7:4]: Drive strength setting, power-on default 0.

Table 15 Timing Interface Speed

Drive Capability Setting	Value	Notes
HS400 Mode	0x3	200MHz DDR Mode
HS200 Mode	0x2	200MHz SDR Mode
HS Mode	0x1	52MHz SDR and DDR Modes
Compatible Mode	0x0	26MHz SDR Mode

Table 16 Drive Strength Setting

Drive Capability Setting	Support Status	Impedance	**Type-0 Reference**	Notes
0x0	Mandatory	50Ω	x1	Default driver type, supports up to 200MHz operation
0x1	Optional	33Ω	x1.5	Supports up to 200MHz operation
0x2	Optional	66Ω	x0.75	Weakest driver supporting up to 200MHz operation; suitable for low-noise and low-EMI systems. Max. operating frequency is determined by host design
0x3	Optional	100Ω	x0.5	
0x4	Optional	40Ω	x1.2	

4.4.3 BUS_WIDTH [183]

Table 17 Bus Mode

Value	Bus Mode
255–7	Reserved
6	8-bit Data Bus DDR
5	4-bit Data Bus DDR
4-3	Reserved
2	8-bit Data Bus SDR
1	4-bit Data Bus SDR
0	1-bit Data Bus SDR

Defaults to 0 (1-bit data bus) after power-up and can be changed by the SWITCH command (CMD6). HS_TIMING must be set to 0x1 before BUS_WIDTH can be set to double data rate mode (0x5 or 0x6).

4.4.4 RST_n_FUNCTION [162]

Table 18 Reset

bit7	bit6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved						RST_n_ENABLE	

bit[7:2]: Reserved

bit[1:0]: RST_n_ENABLE (write-once)

0x0: Temporarily disable RST_n signal (default)

0x1: Permanently enable RST_n signal

0x2: Permanently disable RST_n signal

0x3: Reserved

For backward compatibility, the RST_n signal is temporarily disabled by default at the factory. The host can set this signal to permanently enabled or permanently disabled before using the device.

Generally, the host sets the RST_n_ENABLE bit to 0x2 (permanently disabled), and the device will permanently ignore RST_n signal input. While disabled, any state of the external RST_n (high, low, or floating) will not cause any device problems (such as malfunction or large leakage current in the input buffer).

When RST_n_ENABLE is set to 0x1 (permanently enabled), the device permanently accepts RST_n input. The host cannot change this bit back to the disabled value. In addition, when the host sets RST_n_ENABLE to 0x1, the device must not trigger an internal circuit reset due to a register change. The internal reset sequence must be triggered by the rising edge of the external RST_n pin, not by a register change.

When not configured, since the eMMC internal RST_n signal has no pull-up or pull-down resistor, the host must pull RST_n high or low to avoid unnecessary leakage current in the input circuit when RST_n is enabled.

4.5 RCA Register

The RCA register is the Device Relative Address (RCA) register; it is a 16-bit register. During device identification, the host assigns the device address. This address is used for addressing communication after the device identification routine. The default value of the RCA register is 0x0001. The value 0x0000 is reserved for setting all devices to Stand-by state with CMD7.

4.6 DSR Register

The DSR register is the Device Stage Register; it is a 16-bit register. This register is optional and can be used to extend operating conditions to improve bus performance (depending on parameters such as bus length, transfer rate, or number of devices).

The default value of the DSR register is 0x404.

5 eMMC Partitions

The eMMC initial partitions are mainly divided into 4 parts: the user data area, the RPMB partition and two boot areas.

Two boot areas: These two areas can store system-related information, such as the boot image and default configuration parameters.

RPMB partition: An RPMB partition that can be accessed through a trusted mechanism, used by the system to store special data that requires access authorization.

User data area: This area can be accessed directly by the user and is the actual capacity visible to the eMMC.

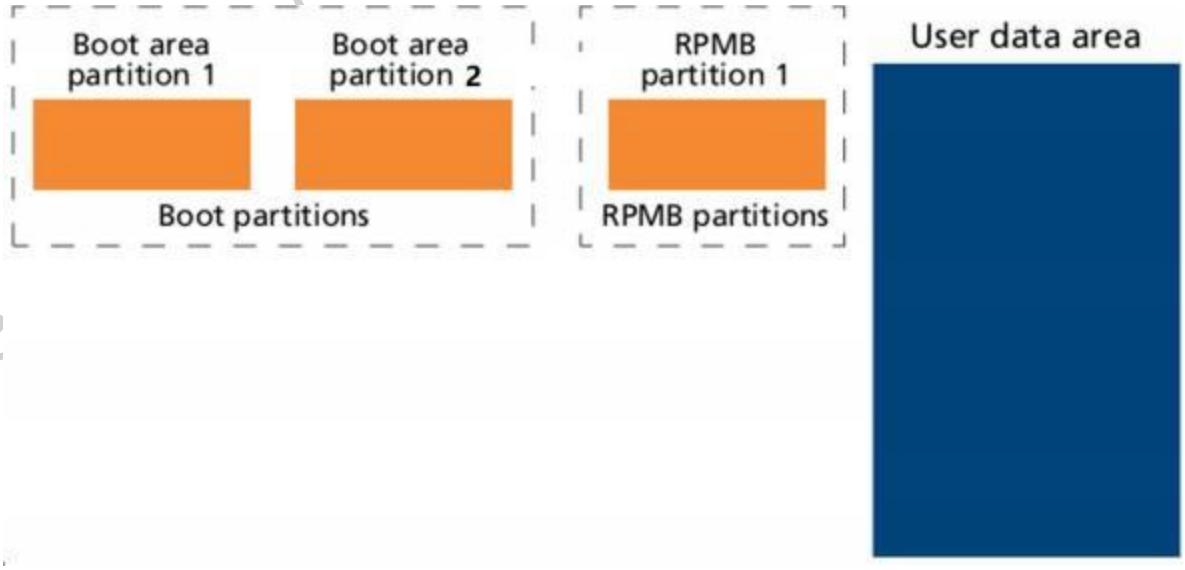


Figure 4 eMMC Partitions

Table 19 Boot Area

	Boot Area 1 Size	Boot Area 2 Size	RPMB Area Size
Default Value	4096KB	4096KB	4096KB
Max.	4096KB	4096KB	4096KB

6 Operating Modes

The five operating modes of eMMC: Boot mode, Card identification mode, Interrupt mode, Data transfer mode, and Inactive mode.

6.1 Boot mode

After power-on, if the eMMC receives CMD0 (GO_Idle_State) with the argument "0xF0F0F0F0", it will enter Boot Mode if Boot mode is supported; otherwise it will enter identification mode. The device supports normal boot mode and alternative boot mode, and the boot process supports high-speed timing and dual data rate modes.

The Boot mode flow is as follows:

- When the system is powered on, hardware reset, or the host issues CMD0 with 0xF0F0F0F0, the system enters Pre-Idle State.

- The device automatically checks whether BOOT_PARTITION_ENABLE is 1. If it is 0, the device exits Boot mode and enters Card-identification Mode. If it is 1, the device proceeds to the next step, pre-boot state.

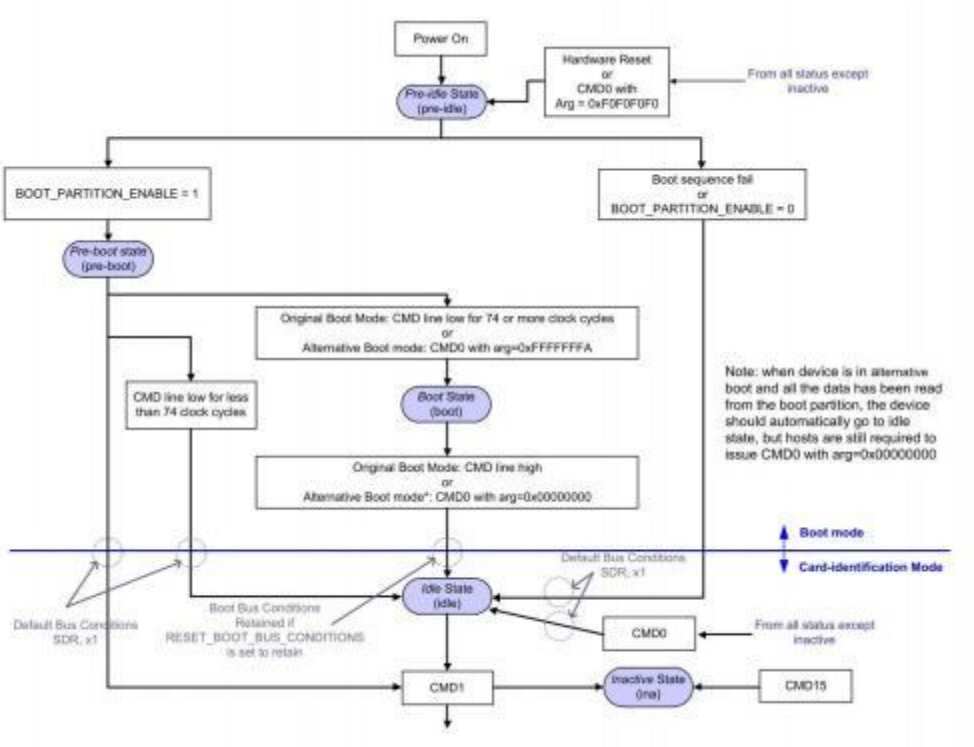


Figure 5 Boot Mode Flow Chart

- The CMD line must be held low for at least 74 clock cycles, or the host sends CMD0 with 0xFFFFFFFA; then the device sends out the data the host wants to read. After the host finishes receiving, it jumps to the Idle State of Card-identification Mode. Otherwise, if the low time is less than 74 clock cycles, Boot mode ends and the device enters the Idle State of Card-identification Mode.

6.2 Card identification mode

After power-on, whether Boot mode completes or is not supported, the Card will enter this mode and wait continuously to receive CMD3 (Send_Relative_Address) from the Host.

For the eMMC to work properly, the initialization process must be completed first. During initialization, the system identifies the eMMC, determines the operating voltage range and usage mode of the device, and assigns an address (RCA) to the device (a system may have multiple eMMCs). This process is called Card identification mode; during initialization, all data communication takes place only on the CMD signal line. The figure below shows the device initialization flow:

The initialization flow is as follows:

- The first step is for the device to enter Idle State. There are two ways to enter Idle State: one is through Power On (power-on entry), and the other is through CMD0 with the argument 0x00000000; CMD0 is a no-response command.

- The second step is for the device to enter Ready State. Ready State is entered through CMD1: only after sending CMD1 with the OCR-format voltage parameter to the MMC, receiving a response with matching voltage and the highest busy bit of the response set to 1, does it indicate the device is idle and enters Ready State. If the voltage parameter of CMD1 received by the MMC does not match, the device enters Inactive State and will not respond to any subsequent process. If the Host's IO voltage is adjustable, the OCR must be read before adjustment. To prevent the device from mistakenly entering Inactive State, CMD1 without arguments can be sent to the MMC, so that only the OCR register is obtained without changing the device state. During identification, the Host cannot change the voltage range; if modification is needed, the identification process must be restarted after the modification.

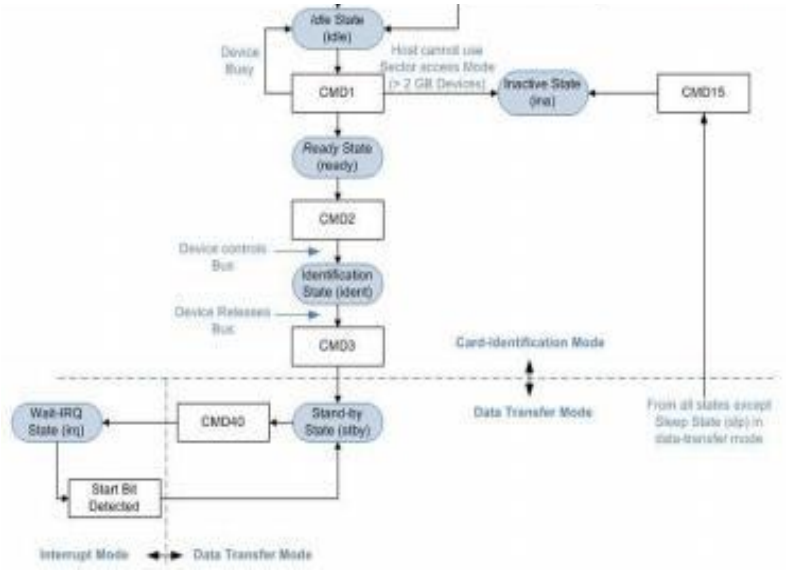


Figure 6 Initialization Flow

- In Ready State, sending CMD2 makes the MMC card enter Identification State.

If CMD2 is sent successfully, the Host obtains the value of the CID register, and the MMC enters Identification

State. If unsuccessful, the device state remains unchanged. In the case of single MMC identification, as long as fop is within range and the pull-up is correct, the CID value should be received accurately, and the device enters Identification State.

- After that, the host sends CMD3 (SET_RELATIVE_ADDR) to assign the device a relative device address (RCA), which will be used to address the device in the next data transfer mode (typically at a clock rate higher than fop). Once the RCA is received, the device enters Stand-by state and no longer responds to further identification cycles. Moreover, the device switches its output driver from open-drain to push-pull.

6.3 Data transfer mode

When the card receives the RCA given by the Host, the device enters Data transfer mode and waits for read/write commands. In this mode, programming of the eMMC, configuration of memory area attributes, data read/write, erase, bus testing, and other functions can be implemented; it is the core mode of eMMC. Two common operations in Data transfer mode:

Read operations (single-block and multi-block);

Write operations (single-block and multi-block).

Single-Block Read Flow:

- When the device is in Stand-by mode, the host sends CMD7 to select the current device, and the device enters transfer state;

- Send CMD16 SET_BLOCKLEN to set the read block length, and wait for the command response;

- Send CMD17 READ_SINGLE_BLOCK single-block read command, and wait for the command response to start reading data;

- The device sends one data block of data; read complete.

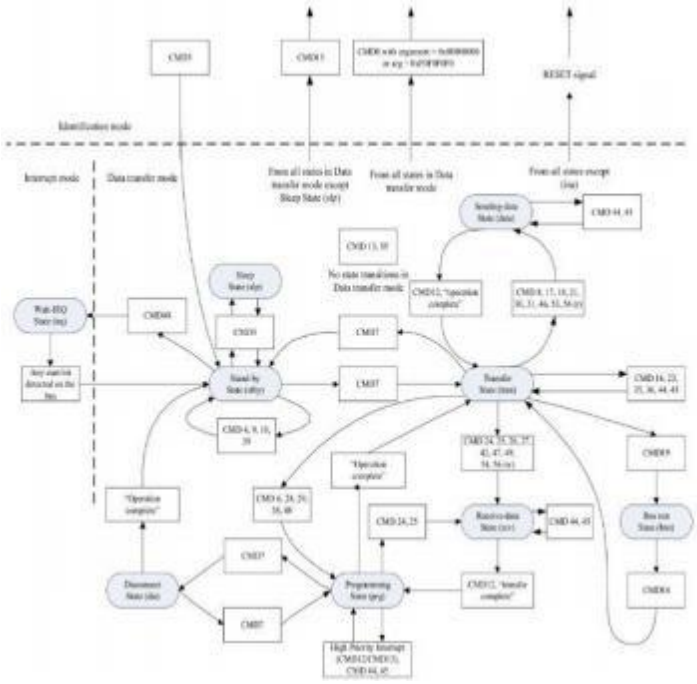


Figure 7 Data Transfer Mode Flow

Single-Block Write Flow

- When the device is in Stand-by mode, the host sends CMD7 to select the current device, and the device enters transfer state;

- Send CMD16 SET_BLOCKLEN to set the read block length, and wait for the command response;

- Send CMD24 WRITE_BLOCK single-block write command;

- Send one data block of data to complete the single-block write operation.

For other operations, refer to JEDEC Standard No.84-B51, Chapter 6.6.

6.4 Interrupt mode

The Host and the device enter this mode at the same time. In this mode, no Data Transfer is performed; only the Host or Card is allowed to send an interrupt service request.

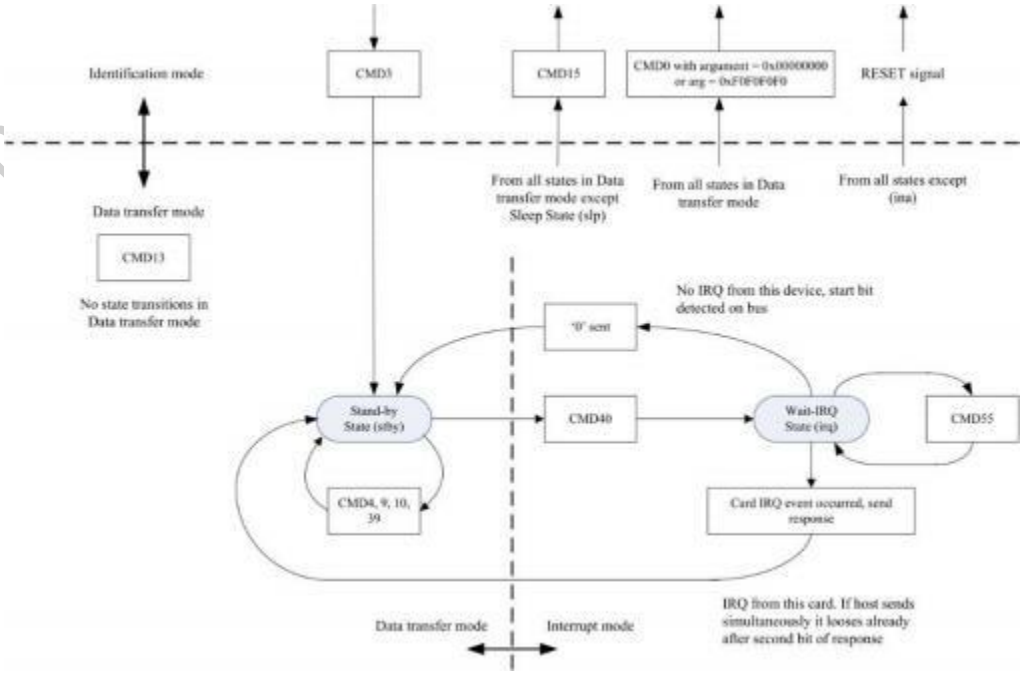


Figure 8 Interrupt Mode

For Interrupt mode related operations, refer to JEDEC Standard No.84-B51, Chapter 6.5.

6.5 Inactive mode

When a Card's voltage does not comply with the specification or the insertion method is invalid, it will enter this mode; the CMD15 command can also be used to put an identified Card into the inactive state.

7 Electrical Characteristics

7.1 General Operating Conditions

Table 20 General Operating Conditions

Parameter	Min.	Max.	Unit	Description
Peak Voltage on All Signal Pins	-0.5	VCCQ + 0.5	V	-
Input Leakage Current (pre-init)	-100	100	μA	-
Input Leakage Current (post-init)	-2	2	μA	-
Output Leakage Current (pre-init)	-100	100	μA	-
Output Leakage Current (post-init)	-2	2	μA	-

7.2 Power Supply Range

Table 21 Power Supply Range

Identification Parameter	Description	Min.	Typ.	Max.	Unit
VCC	NAND FLASH Core Supply	2.7	3.3	3.6	V
VCCQ	NAND FLASH and Controller IO Supply	2.7/1.7	3.3/1.8	3.6/1.95	V

7.3 Bus Load

Table 22 Bus Load

Parameter	Symbol	Min.	Typ.	Max.	Unit	Description
CMD Pull-up Resistor	RCMD	4.7	--	100	kΩ	External Pull-up to VCCQ
DAT0-7 Pull-up Resistor	RDAT	10	--	100	kΩ	External Pull-up to VCCQ
DAT1-7 Internal Pull-up Resistor	Rint	10	--	150	kΩ	Prevent floating of unconnected lines
Bus Capacitance	C_L	--	--	30	pF	Single Device
Device Capacitance	CDEVICE	--	--	12	pF	Single Device capacitance
Signal Inductance	--	--	--	16	nH	fPP≤52MHz

Note: For 1.8V VCCQ interface, the recommended maximum pull-up resistor is 50k ohm; for 3.3V interface, up to 100k ohm is supported.

The total capacitance CL of each line of the eMMC bus is the sum of the host capacitance CHOST, the bus capacitance CBUS itself, and the capacitance CDEVICE of the eMMC connected to the line: CL = CHOST + CBUS + CDEVICE.

7.4 Bus Signal Levels

Since the supply voltage is a variable value, the levels of all bus signals are related to the supply voltage.

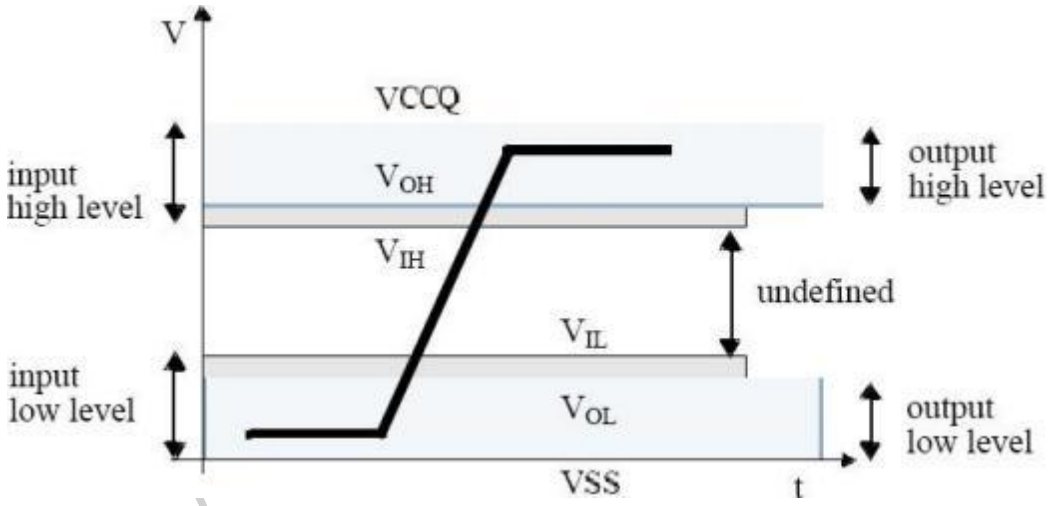


Figure 9 Bus Levels

7.4.1 Open-Drain Mode Bus Levels

Table 23 Open-Drain Mode Bus Levels

Parameter	Symbol	Min.	Max.	Unit	Description
Output High Voltage	V_{OH}	VCCQ-0.2		V	Note
Output Low Voltage	V_{OL}		0.3	V	I_{OL}=2mA

Note: VOH depends on the external pull-up resistor value. VCCQ supports 3.3V and 1.8V supplies; in open-drain mode, the level follows the VCCQ reference.

7.4.2 Push-Pull Mode Bus Levels

After initialization, the bus switches to push-pull mode, available in two specifications: 3.3V signaling and 1.8V signaling:

- 3.3V Signaling Mode (for compatible mode / HS mode)

Table 24 Push-Pull Mode 3.3V Signaling Bus Levels

Parameter	Symbol	Min.	Max.	Unit	Description
Output High Voltage	V_{OH}	0.75 * VCCQ		V	IOH = -100μA @ VCCQ min.
Output Low Voltage	V_{OL}		0.125 * VCCQ	V	IOL = 100μA @ VCCQ min.
Input High Voltage	VIH	0.625 * VCCQ	VCCQ + 0.3	V	
Input Low Voltage	VIL	VSS - 0.3	0.25 * VCCQ	V	

- 1.8V Signaling Mode (for HS200/HS400 high-speed modes)

Table 25 Push-Pull Mode 1.8V Signaling Bus Levels

Parameter	Symbol	Min.	Max.	Unit	Description
Output High Voltage	V_{OH}	VCCQ - 0.45		V	IOH = -2 mA
Output Low Voltage	V_{OL}		0.45	V	IOL = 2 mA
Input High Voltage	VIH	0.65 × VCCQ	VCCQ + 0.3	V	
Input Low Voltage	VIL	VSS - 0.3	0.35 × VCCQ	V	

7.5 Power-up Timing

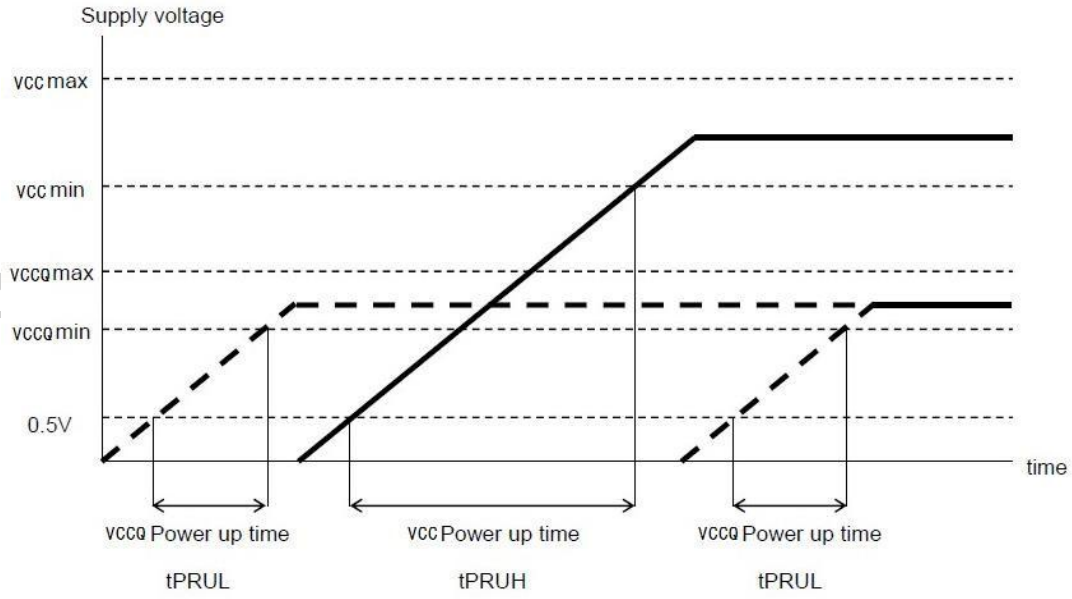


Figure 10 Power-up Timing

Table 26 Power-up Parameters

Parameter	Symbol	Min.	Max.	Description
VCC=3.3V	tPRUH	5μs	35ms	--
VCCQ=1.8V	tPRUL	5μs	25ms	--

There is no sequence requirement for the eMMC power supplies, but there are certain requirements for the ramp-up time of each supply, as detailed above. Failure to meet the power supply ramp-up time may cause unrecognized or intermittently unrecognized issues.

7.6 Recommended Circuit Capacitance

Table 27 Recommended Circuit Capacitance

Parameter	Min.	Typ.	Max.	Unit
VCC	10		47	uF
VCCQ	10		47	uF
VDDi	0.1		2.2	uF

7.7 eMMC Bus Timing in Backward-Compatible and High-Speed Modes

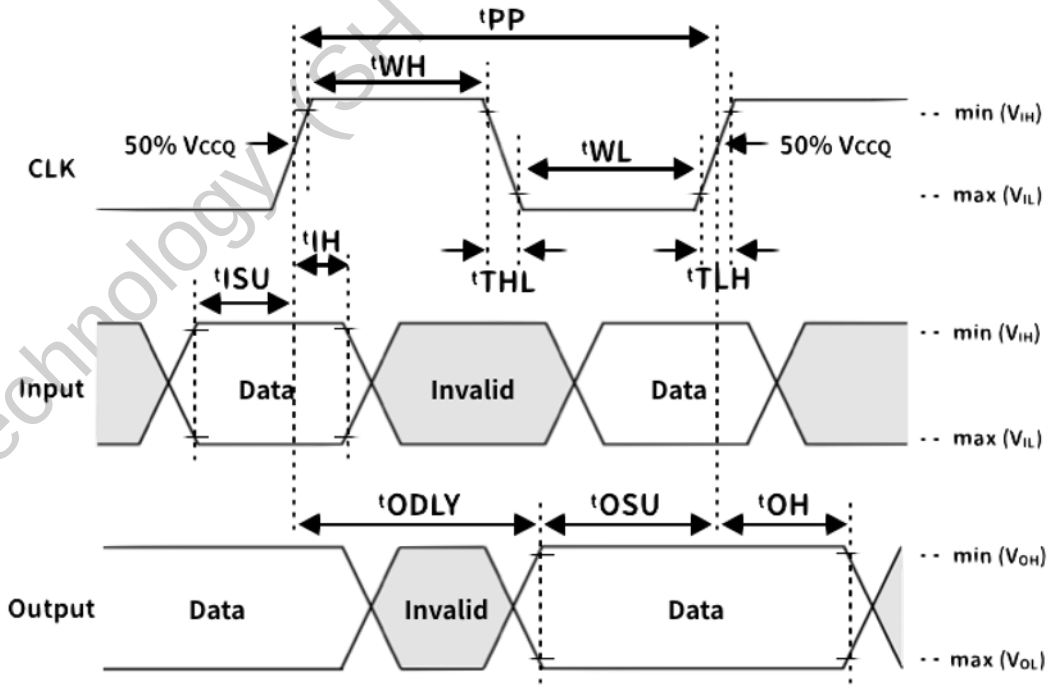


Figure 11 Data Input/Output Timing Diagram (referenced to clock)
(eMMC Backward-Compatible and High-Speed Modes)

Table 28 eMMC Backward-Compatible Mode Timing Parameters

Parameter	Symbol	Min.	Max.	Unit	Notes
Input MMC_CLK					
Data Transfer Mode Clock Frequency	f_{pp}	0	26	MHz	C_L<30pF
Identification Mode Clock Frequency	f_{OD}	0	400	KHz	
Clock Low Time / Clock High Time	t_{WL}/t_{WH}	10	-	ns	C_L<30pF
Clock Rise Time / Clock Fall Time	t_{TLH}/t_{THL}	-	10	ns	C_L<30pF
Input CMD, DAT Signals (referenced to MMC_CLK)					
Input Setup Time	t_{ISU}	3	-	ns	C_L<30pF
Input Hold Time	t_{IH}	3	-	ns	C_L<30pF

Parameter	Symbol	Min.	Max.	Unit	Notes
Output CMD, DAT Signals (referenced to MMC_CLK)					
Output Delay Time	t_{OSU}	11.7	-	ns	C_L<30pF
Output Hold Time	t_{OH}	8.3	-	ns	C_L<30pF

Note:

(1) Clock timing is measured at the 50% level of VCCQ.

(2) Clock rise/fall times are measured with the input high-level minimum (VIH) and input low-level maximum (VIL) as references

Table 29 eMMC High-Speed Mode Timing Parameters

Parameter	Symbol	Min.	Max.	Unit	Notes
Input MMC_CLK [1]					
Data Transfer Mode Clock Frequency	f_{pp}	0	52	MHz	C_L<30pF
Identification Mode Clock Frequency	f_{OD}	0	400	KHz	
Clock Low Time / Clock High Time	t_{WL}/t_{WH}	6.5	-	ns	C_L<30pF
Clock Rise Time / Clock Fall Time	t_{TLH}/t_{THL}	-	3	ns	C_L<30pF
Input CMD, DAT Signals (referenced to MMC_CLK)					
Input Setup Time	t_{ISU}	3	-	ns	C_L<30pF
Input Hold Time	t_{IH}	3	-	ns	C_L<30pF
Output CMD, DAT Signals (referenced to MMC_CLK)					
Output Delay Time	t_{ODLY}	-	13.7	ns	C_L<30pF
Output Hold Time	t_{OH}	2.5	-	ns	C_L<30pF
Signal Rise Time [2]	t_{RISE}	-	3	ns	C_L<30pF
Signal Fall Time	t_{FALL}	-	3	ns	C_L<30pF

Note:

(1) Clock timing is measured at the 50% level of VCCQ.

(2) Clock rise/fall times are measured with the input high-level minimum (VIH) and input low-level maximum (VIL) as references.

(3) The rise/fall times of CMD and DAT input signals are measured with (VIH) min and (VIL) max as references; the rise/fall times of CMD and DAT output signals are measured with (VIH) min and (VIL) max as references.

7.8 eMMC Bus Timing in DDR Mode

Figure 12 Data Input/Output Timing Diagram (referenced to clock, DDR mode)

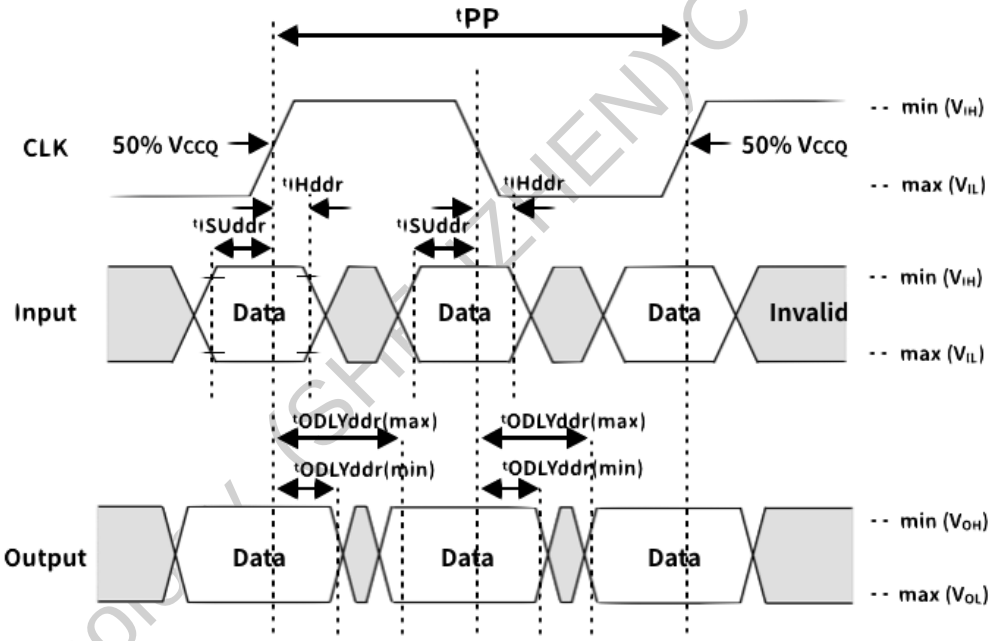


Table 30 eMMC DDR Mode Timing Parameters

Parameter	Symbol	Min.	Max.	Unit	Notes
Input MMC_CLK					
Clock Duty Cycle	-	45	55	%	
Clock Rise Time / Clock Fall Time	t_{TLH}/t_{THL}	-	3	ns	C_L<30pF
Input CMD Signal (referenced to MMC_CLK)					
Input Setup Time	t_{ISUddr}	3	-	ns	C_L<20pF
Input Hold Time	t_{IHddr}	3	-	ns	C_L<20pF
Output CMD Signal (referenced to MMC_CLK)					
Data Transfer Output Delay Time	t_{ODLY}	-	13.7	ns	C_L<20pF
Output Hold Time	t_{OH}	2.5	-	ns	C_L<20pF
Signal Rise Time	t_{RISE}	-	3	ns	C_L<20pF
Signal Fall Time	t_{FALL}	-	3	ns	C_L<20pF
Input DAT Signal (referenced to MMC_CLK)					
Input Setup Time	t_{ISUddr}	2.5	-	ns	C_L<20pF
Input Hold Time	t_{IHddr}	2.5	-	ns	C_L<20pF
Output DAT Signal (referenced to MMC_CLK)					
Data Transfer Output Delay Time	$t_{ODLYddr}$	1.5	7	ns	C_L<20pF
Signal Rise Time	t_{RISE}	-	2	ns	C_L<20pF
Signal Rise Time	t_{FALL}	-	2	ns	C_L<20pF

Note:

(1) Clock timing is measured at the 50% level of VCCQ.

(2) The rise/fall times of DAT input signals are measured with (V_IH) min and (V_IL) max as references; the rise/fall times of DAT output signals are measured with (V_OH) min and (V_OL) max as references.

7.9 eMMC Bus Timing in HS200 Mode

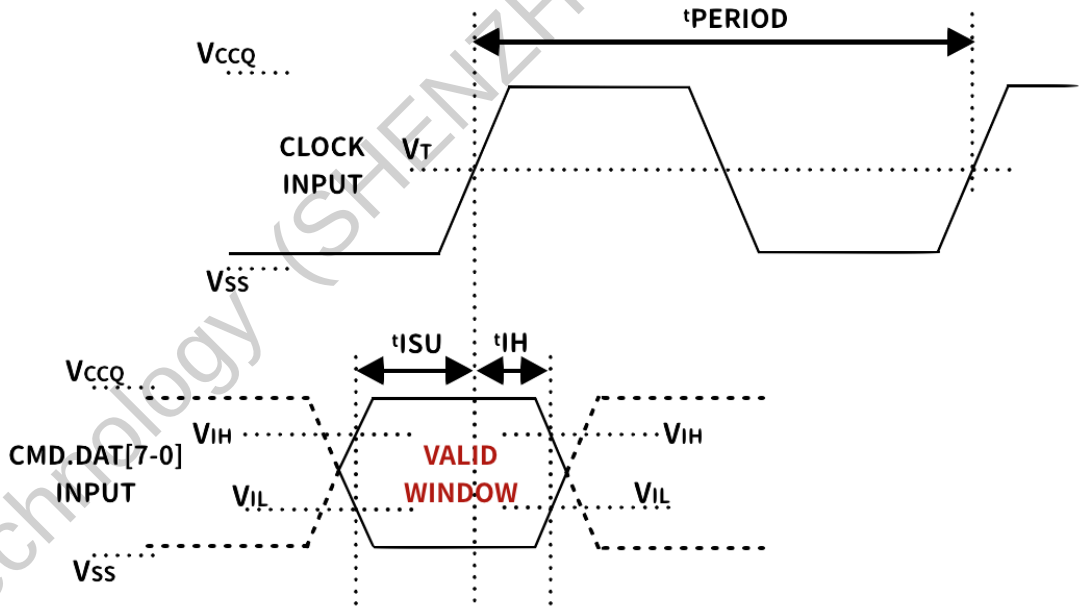


Figure 13 Data Input Timing Diagram (referenced to clock, HS200 mode)

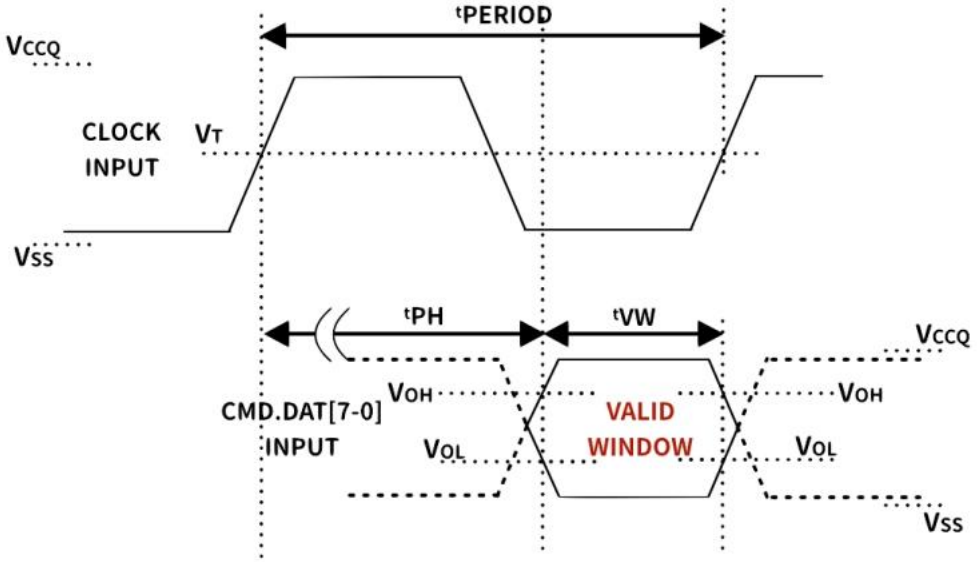


Figure 14 Data Output Timing Diagram (referenced to clock, HS200 mode)

Table 31 eMMC HS200 Mode Timing Parameters

Parameter	Symbol	Min.	Max.	Unit	Notes
Input Clock MMC_CLK					
Clock Cycle	t_{PERIOD}	5	-	ns	
Clock Rise Time / Clock Fall Time	t_{TLH}/t_{THL}	-	1	ns	C_{Device}=6pF
Clock Duty Cycle	-	30	70	%	
Input CMD, DAT Signals (referenced to MMC_CLK)					
Input Setup Time	t_{ISU}	1.4	-	ns	C_{Device}≤6pF
Input Hold Time	t_{IH}	0.8	-	ns	C_{Device}≤6pF
Output CMD, DAT Signals (referenced to MMC_CLK)					
Data Transfer Output Delay Time	t_{PH}	0	2	UI	
Delay Deviation from Temp. Change After Calibration	Δ_{TPH}	-350 (ΔT=-20℃)	+1550 (ΔT=90℃)	ps	
Signal Rise Time	t_{VW}	0.575	-	UI	

Note: The unit interval (UI) is the nominal duration of 1 bit, e.g., UI = 5ns at 200MHz clock.

7.10 eMMC Bus Timing in HS400 Mode

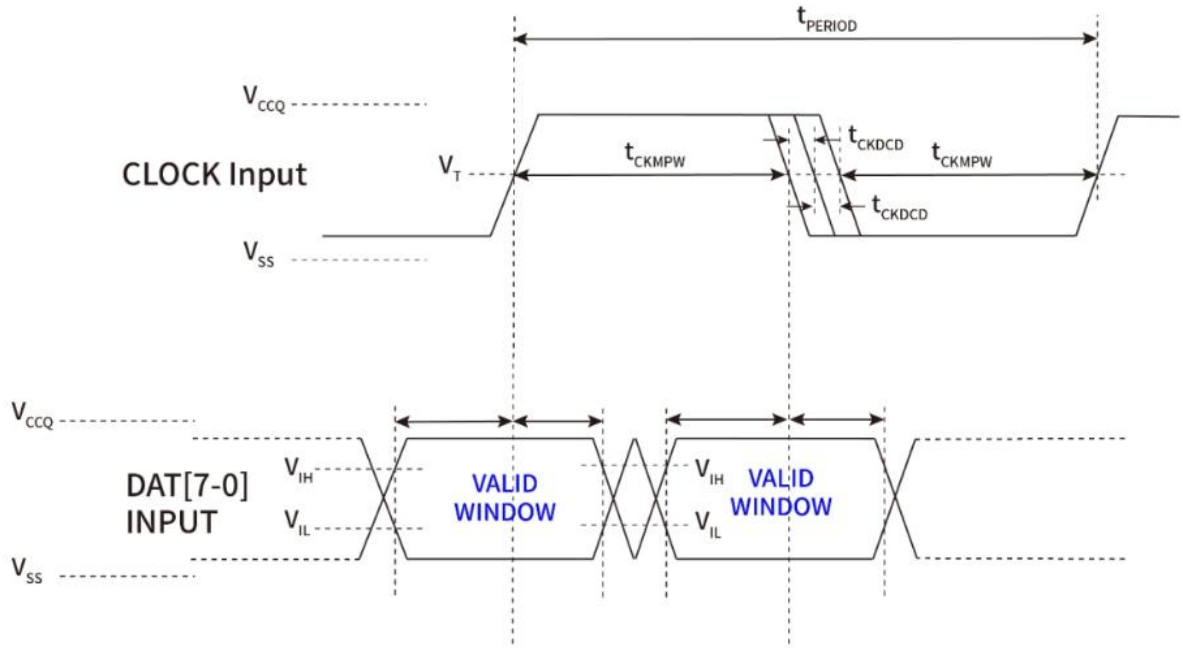


Figure 15 Data Input Timing Diagram (referenced to clock, HS400 mode)

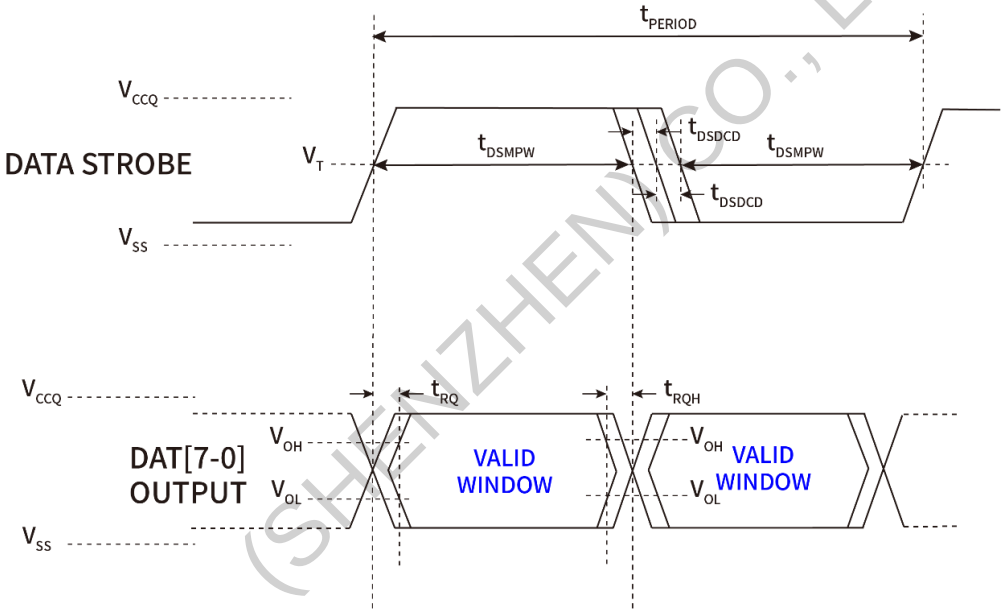


Figure 16 Data Output Timing Diagram (referenced to data strobe, HS400 mode)

Table 32 eMMC HS400 Mode Timing Parameters

Parameter	Symbol	Min.	Max.	Unit	Notes
Input MMC_CLK					
Clock Cycle	t_{PERIOD}	5	-	ns	
Slew Rate	SR	1.125	-	V/ns	
Duty Cycle Distortion	t_{CKDCD}	0	0.3	ns	
Min. Pulse Width	t_{CKMPW}	2.2	-	ns	
Input DAT Signal (referenced to MMC_CLK)					
Input Setup Time	t_{ISUddr}	0.4	-	ns	C_{Device}≤6pF
Input Hold Time	t_{IHddr}	0.4	-	ns	C_{Device}≤6pF
Slew Rate	SR	1.125		V/ns	
Output Data Strobe (DS) Signal					
Clock Cycle	t_{PERIOD}	5	-	ns	
Slew Rate	SR	1.125	-	V/ns	
Duty Cycle Distortion	t_{CKDCD}	0	0.2	ns	
Min. Pulse Width	t_{CKMPW}	2	-	ns	
Read Preamble	t_{RPRE}	0.4	-	t_{PERIOD}	
Read Postamble	t_{RPST}	0.4	-	t_{PERIOD}	
Output DAT/CMD Signal (referenced to data strobe)					
Output Skew	t_{RQ}/t_{RQ_CMD}	-	0.4	ns	
Output Hold Skew	t_{RQH}/t_{RQH_CMD}	-	0.4	ns	
Slew Rate	SR	1.125	-	V/ns	

8 Recommended Design

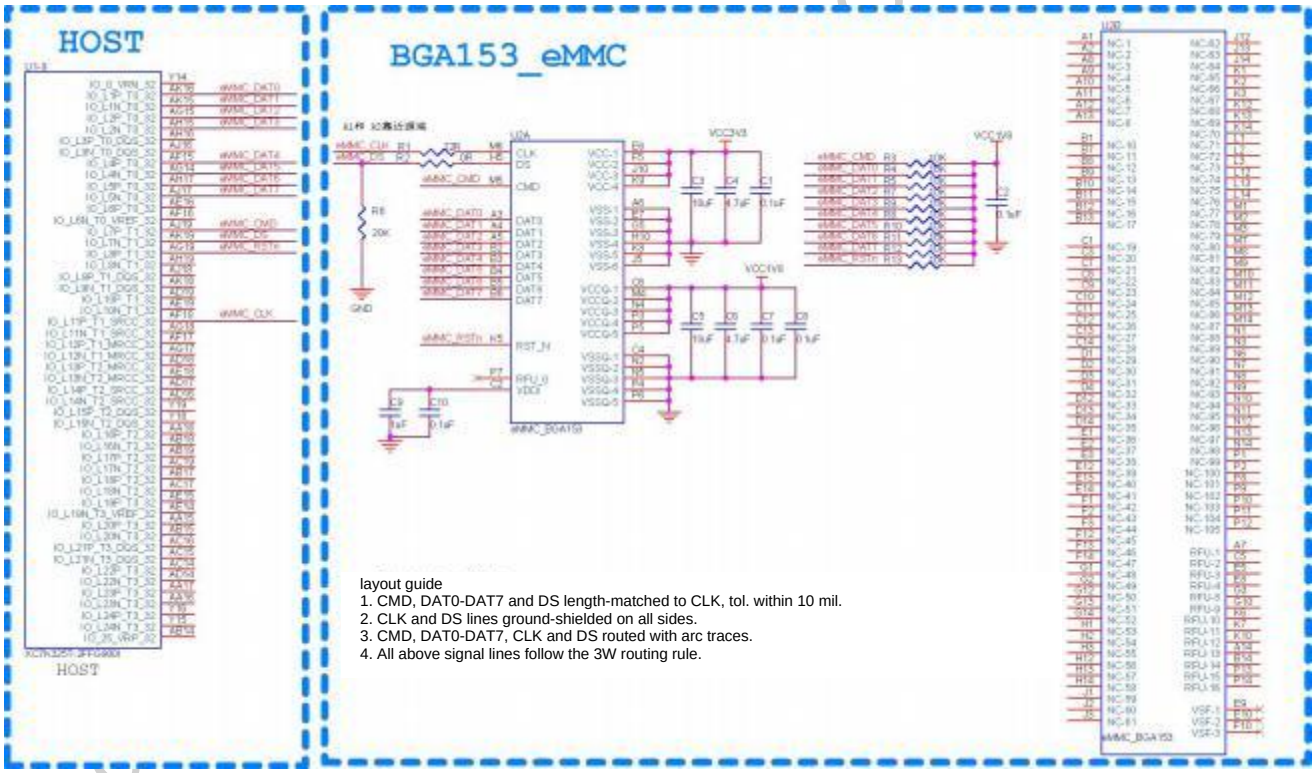


Figure 11 Reference Design (153-ball)

1. Filter capacitors should be placed as close as possible to the VCC/VCCQ and VSS pins.

2. The eMMC_IO supply voltage depends on the host eMMC interface and the user's actual usage mode, but must be consistent with the host IO level. Level-shifting chips are prohibited to prevent read/write errors caused by the delay of level-shifting chips in high-speed operating modes.

3. It is recommended to pour ground between CLK and DATA lines in layout.

4. Unused IOs can be disconnected from the Host; their pull-up resistors should be retained according to the reference schematic above.

5. The recommended minimum decoupling capacitor for the VDDi pin is 1uF.

6. It is recommended to route VCC and VCCQ power paths separately to reduce high-speed signal interference.

7. It is recommended to series-connect a 0-ohm resistor (default) on the clock signal line, adjustable within 0-100 ohm, for signal integrity matching.

9 Soldering Process

Chips must be baked at 125C (+10C/-0C) with humidity below 5% for 9 hours before soldering.

Select the corresponding soldering process parameters according to the soldering process; the reflow profile can refer to the figure below, and the reflow profile parameters can be set according to the table below. The reflow profile settings should be comprehensively considered in combination with the solder paste and the parameters of other chips on the product. The peak reflow temperature of the device package is 260C, and the maximum time at peak temperature 250C-260C is 20s.

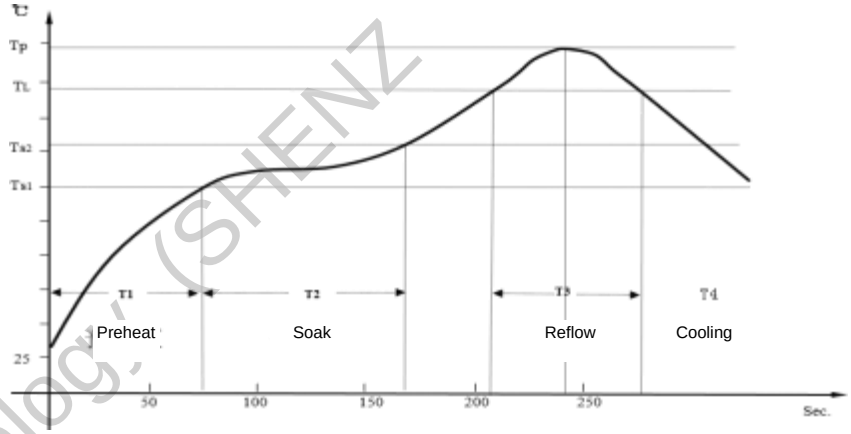


Figure 12 Reflow Soldering Curve

Table 33 Reflow Soldering Parameters

Curve Item	Leaded Alloy Curve	Leaded Mixed Curve	Lead-Free Alloy Curve
Liquidus Temperature (TL)	183℃	183℃/220℃	220℃
Peak Temperature Range (Tp)	210℃-225℃	230℃-235℃	235℃-250℃
Min. Reflow Peak Temperature (Tp)	205℃	230℃	230℃
Ramp-up Rate (T1)	1.5℃/s-3℃/s	1.5℃/s-3℃/s	1.5℃/s-3℃/s
Ramp-down Rate (T4)	2℃/s-5℃/s	2℃/s-5℃/s	2℃/s-5℃/s
Soak Temperature (T2)	120℃-160℃	120℃-160℃	150℃-180℃
Soak Time (T2)	60s-100s	60s-100s	60s-100s
Time Above Liquidus (T3)	60s-90s	60s-120s	60s-90s

10 Miscellaneous

Customization services are available; please contact us if needed.

The product manual is subject to upgrade without prior notice. If there is any discrepancy between the datasheet and the actual product, please contact the manufacturer for the latest information.