eMMC 5.1 Datasheet

PS32GAAJS-00N0

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PRODUCT LIST:

Specifications	FLASH	BUS	VCC	Packaging
PS32GAAJS-00N0	32GB	X8	3.3V	FBGA153

Revision History

Revision	Date	Description
Rev 1.0	2025/06/19	Create new document

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1. INTRODUCTION

PS32GAAJS-00N0 is an embedded MultiMediaCard (MMC) controller and 32GB NAND Flash PS32GAAJS-00N0 offers space saving advantage that could miniaturize your portable device, and it is conformed with Green regulations.

1.1 Application

- Compact DSC / CAR Black Box / Action Cam / 360 Cam
- Drone
- Wearable

1.2 Features

PRODUCT LIST

●PS32GAAJS-00N0

■ JEDEC/MMC standard version 5.0/5.1 compatible (backward compatible to eMMC 4.5)

POWER SUPPLY

- eMMC
  - ■ V_{CC}: 3.3V (2.7-3.6V)
  - ■ V_{CCQ}: 3.3V (2.7-3.6V) /1.8V (1.7-1.95V)

PACKAGE

- FBGA 11.5 x 13 x 1.0mm, 153 Balls
- Ball Pitch: 0.5mm
- Weight: TBD

Temperature

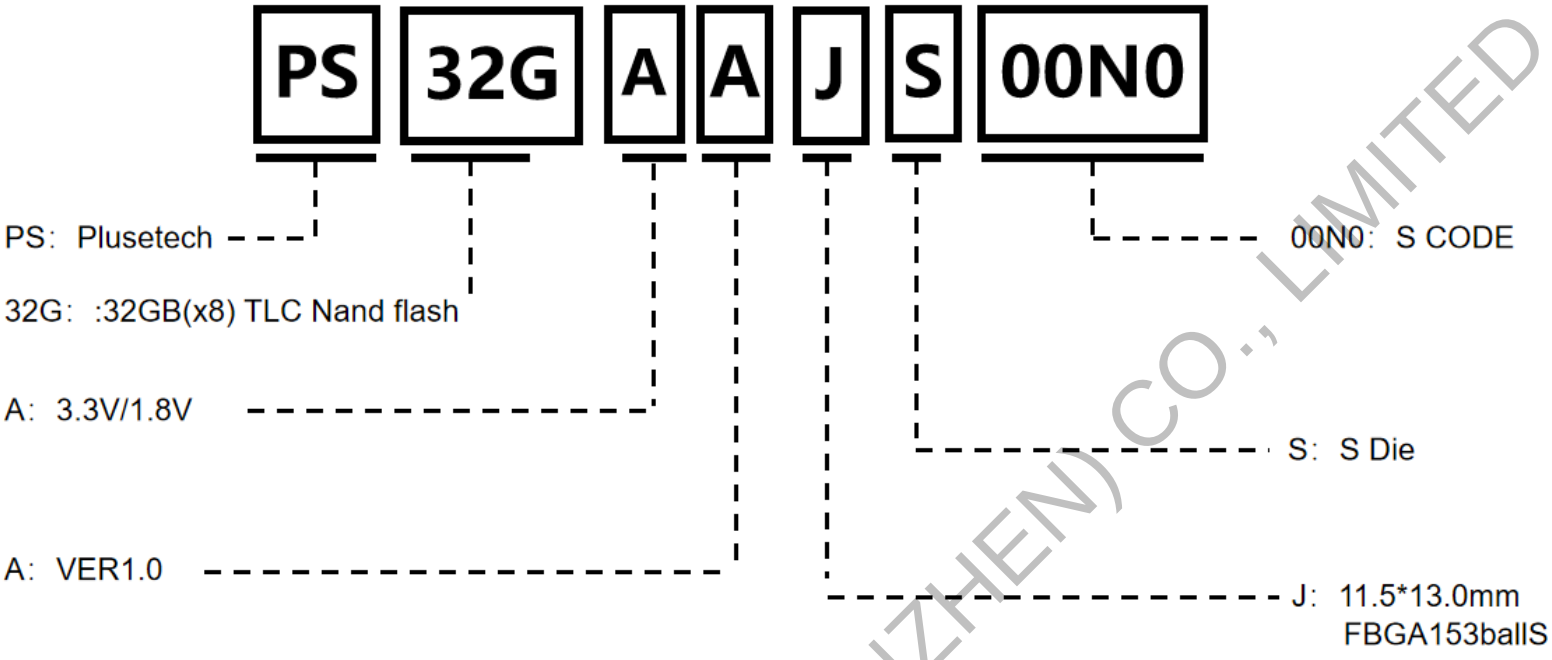
- Operating: -25 to + 85°C
- Storage: -65 to +100°C

eMMC-Specific Features

- embedded MultiMediaCard Ver. 5.1 compatible.
- eMMC supports features of eMMC5.1 which are defined in JEDEC Standard
  - Major Supported Features: HS400, Field Firmware Update, Cache, Command Queuing, Enhanced Strobe Mode, Secure Write Protection, Partition types.
  - Non-supported Features: Large Sector Size (4KB)
- Backward compatibility with previous MultiMediaCard system specification (1bit data bus, multi-eMMC systems)
- Data bus width: 1bit (Default), 4bit and 8bit
- MMC I/F Clock Frequency: 0 ~ 200MHz
  MMC I/F Boot Frequency: 0 ~ 52MHz
- Power: Interface power → VCCQ (2.7V ~ 3.6V)/ (1.7V ~ 1.95V), Memory power → VCC (2.7V ~ 3.6V)

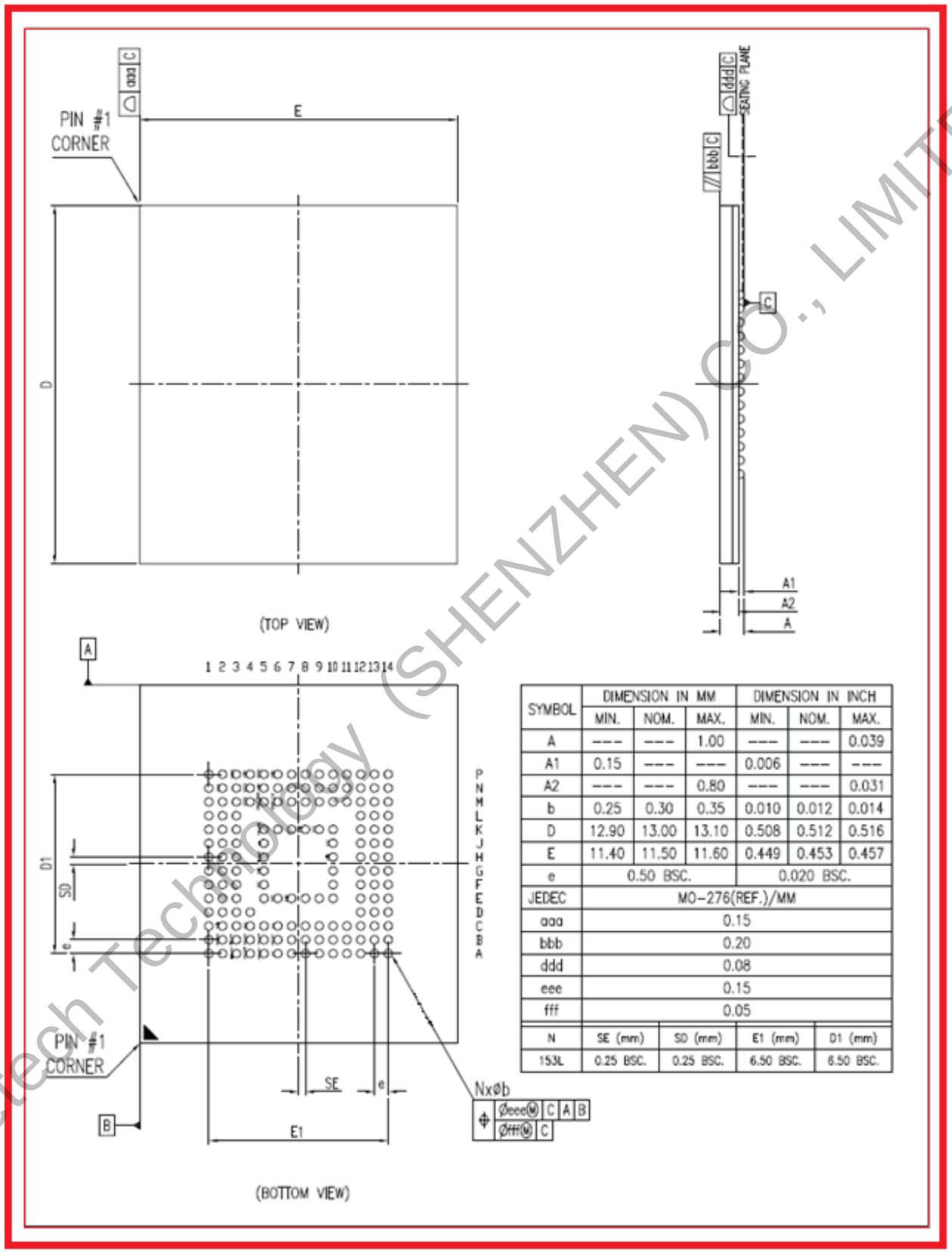
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2. PART NUMBER LOGIC:



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3. PACKAGE DIMENSION (153Ball FBGA, 11.5x13x1.0mm)



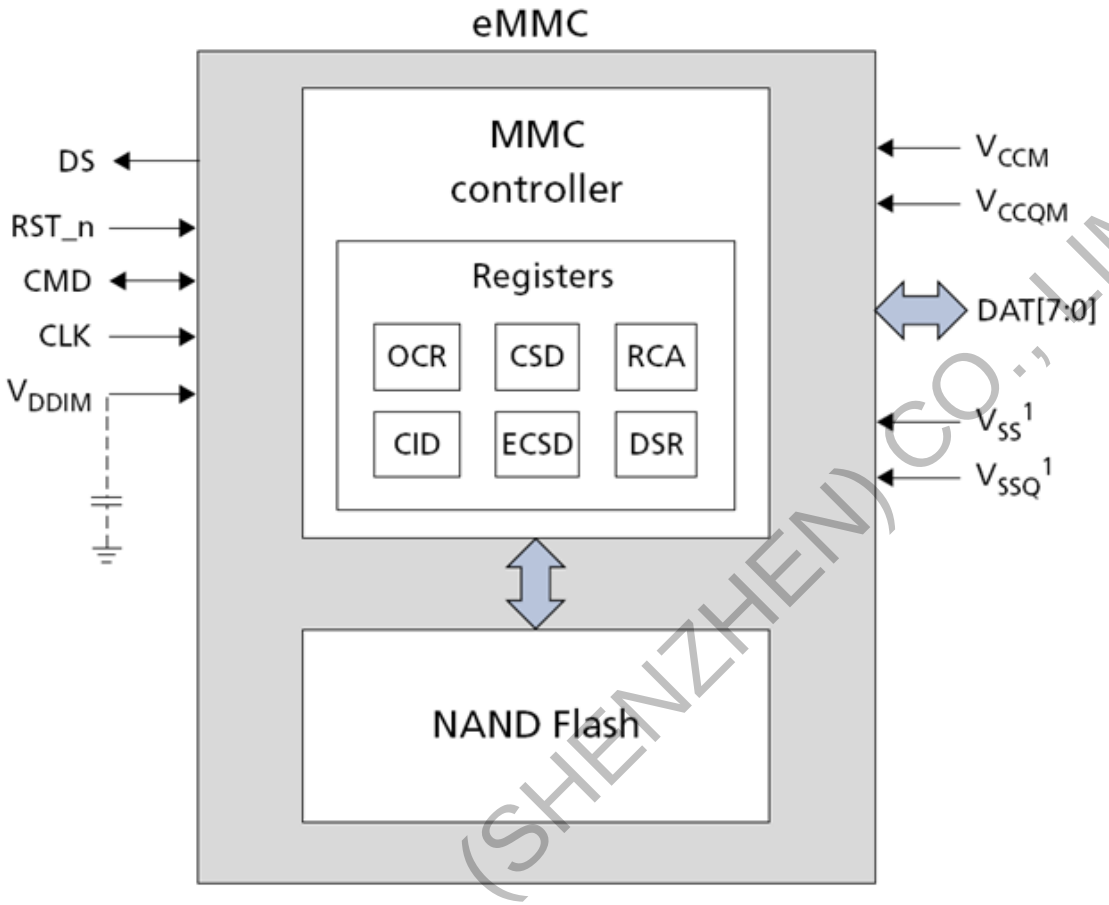
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.00	---	---	0.039
A1	0.15	---	---	0.006	---	---
A2	---	---	0.80	---	---	0.031
b	0.25	0.30	0.35	0.010	0.012	0.014
D	12.90	13.00	13.10	0.508	0.512	0.516
E	11.40	11.50	11.60	0.449	0.453	0.457
e	0.50 BSC.			0.020 BSC.		
JEDEC	MO-276(REF.)/MM					
aaa	0.15					
bbb	0.20					
ddd	0.08					
eee	0.15					
fff	0.05					

N	SE (mm)	SD (mm)	E1 (mm)	D1 (mm)
153L	0.25 BSC.	0.25 BSC.	6.50 BSC.	6.50 BSC.

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4. FUNCTION DIAGRAM

4.1 eMMC



Note:

1. V_{SS} and V_{SSQ} are internally connected.

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5. PIN CONFIGURATION

5.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	DAT0	DAT1	DAT2	Vss	RFU	NC	NC	NC	NC	NC	NC	NC
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC
C	NC	VDDIM	NC	VssQ	RFU	VccQ	NC	NC	NC	NC	NC	NC	NC	NC
D	NC	NC	NC	NC (index)								NC	NC	NC
E	NC	NC	NC		RFU	Vcc	Vss	RFU	RFU	RFU		NC	NC	NC
F	NC	NC	NC		Vcc					RFU		NC	NC	NC
G	NC	NC	RFU		Vss					RFU		NC	NC	NC
H	NC	NC	NC		DS					Vss		NC	NC	NC
J	NC	NC	NC		Vss					Vcc		NC	NC	NC
K	NC	NC	NC		RST_n	RFU	RFU	Vss	Vcc	RFU		NC	NC	NC
L	NC	NC	NC									NC	NC	NC
M	NC	NC	NC	VccQ	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC
N	NC	VssQ	NC	VccQ	VssQ	NC	NC	NC	NC	NC	NC	NC	NC	NC
P	NC	NC	VccQ	VssQ	VccQ	VssQ	RFU	NC	NC	RFU	NC	NC	NC	NC

TOP VIEW

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5.2 Pin Descriptions

Type Symbol	Description	Type Symbol	Description
I	Input	P	Power
O	Output	G	Ground
I/O	Bi-direction	X	No connect (No function, don't care)

Symbol	Type	Count	Description
DAT[7:0]	I/O	8	**Data I/O:** These are bidirectional data signals. The DAT signals operate in push-pull mode. By default,after power-on or assertion of the RST_n signal, only DAT0 is used for data transfer. TheMMC controller can configure a wider data bus for data transfer either using DAT[3:0] (4-bit mode)or DAT[7:0] (8-bit mode). The device includes internal pull-up resistors for data lines DAT[7:1]. Immediatelyafter entering the 4-bit mode, the device disconnects the internal pull-up resistors onthe DAT[3:1] lines. Upon entering the 8-bit mode, the device disconnects the internal pull-ups on the DAT[7:1] lines.
CMD	I/O	1	**Command:** This signal is a bidirectional command channel used for command and response transfers.The CMD signal has two bus modes: open-drain mode and push-pull mode. Commands aresent from the MMC host to the device, and responses are sent from the device to the host.
CLK	I	1	**Clock:** Each cycle of the clock directs a transfer on the command line and on the data line(s). Thefrequency can vary between the minimum and the maximum clock frequency.
DS	O	1	**Data strobe:** Generated by the device and used for data output and CRC status response output inHS400 mode. The frequency of this signal follows the frequency of CLK. For data output, each cycleof this signal directs two bits transfer (2x) on the data, one bit for the positive edge and the otherbit for the negative edge. For CRC status response output, the CRC status is latched on the positiveedge only, and is "Don't Care" on the negative edge.
RST_n	I	1	**Reset:** The RST_n signal is used by the host for resetting the device, moving the device to the preidlestate. By default, the RST_n signal is temporarily disabled in the device. The host must set ECSDregister byte 162, bits[1:0] to 0x1 to enable this functionality before the host can use it.
V_{CC}	P	4	**V_{CC}:** NAND interface (I/F) I/O and NAND Flash power supply.
V_{CCQ}	P	5	**V_{CCQ}:** eMMC controller core and eMMC I/F I/O power supply.
V_{DDIM} (V_{DDI_M})	P	1	Internal voltage node. Do not tie to supply voltage or ground.
V_{SS}	G	6	**V_{SS}:** NAND I/F I/O and NAND Flash ground connection.
V_{SSQ}	G	5	**V_{SSQ}:** eMMC controller core and eMMC I/F ground connection.
RFU	X	14	**Reserved for future use:** No internal connection is present. Leave it floatingexternally.
NC	X	106	**No connect:** No internal connection is present.

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6. eMMC

6.1HS400 mode

eMMC 5.0 product supports high speed DDR interface timing mode up to 400MB/s at 200MHz with 1.8V I/O supply.
HS400 mode supports the following features :

- DDR Data sampling method
- CLK frequency up to 200MHz DDR (up to 400Mbps)
- Only 8-bits bus width available
- Signaling levels of 1.8V
- Six selectable Drive Strength (refer to the table below)

Table 4-1 I/O driver strength types

Driver Type	HS200 & HS400 Support	Norminal Impedence	Approximated driving capability compard to Type-0	Remark
0	Default	50Ω	X1	Default Driver Type. Supports up to 200MHz operation.
1	Optional	33Ω	X1.5	Supports up to 200MHz Operation.
2	Optional	66Ω	X0.75	The weakest driver that supports up to 200MHz operation.
3	Optional	100Ω	X0.5	For low noise and low EMI systems. Maximal operating frequency is decided by Host design.
4	Optional	40Ω	X1.2	Supports up to 200MHz DDR operation

Note:

i. Support of Driver Type-0 is default for HS200 & HS400 Device, while supporting Driver types 1~4 are optional for HS200 & HS400 Device

Table 4-2 Device type values (EXT_CSD register: DEVICE_TYPE [196])

Bit	Device Type	Supportablility
7	HS400 Dual Data Rate eMMC @ 200 MHz - 1.2V I/O	Not support
6	HS400 Dual Data Rate eMMC @ 200 MHz - 1.8V I/O	Support
5	HS200 Single Data Rate eMMC @ 200 MHz - 1.2V I/O	Not support
4	HS200 Single Data Rate eMMC @ 200 MHz - 1.8V I/O	Support
3	High-Speed Dual Data Rate eMMC @ 52MHz - 1.2V I/O	Not support
2	High-Speed Dual Data Rate eMMC @ 52MHz - 1.8V or 3V I/O	Support
1	High-Speed eMMC @ 52MHz - at rated device voltage(s)	Support
0	High-Speed eMMC @ 26MHz - at rated device voltage(s)	Support

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Table 4-3 High speed timing values (EXT_CSD register: HS_TIMING [185])

Value	Timing Interface	Supportability
0x0	Selecting backwards compatibility interface timing	Support
0x1	High Speed	Support
0x2	HS200	Support
0x3	HS400	Support

6.2 New eMMC 5.1 Features

Table 4-4 Overviews

New Feature	JEDEC	Support
Cache Flushing Report	Mandatory	Yes
Background operation control	Mandatory	Yes
Command Queuing	Optional	Yes
Enhanced Strobe	Optional	Yes
RPMB Throughput improve	Optional	Yes
Secure Write Protection	Optional	Yes

Command Queuing

To facilitate command queuing in eMMC, the device manages an internal task queue that the host can queue during data transfer tasks.

Every task is issued by the host and initially queued as pending. The device works to prepare pending tasks for execution. When a task is ready for exe - cution, its state changes to “ready for execution”.

The host tracks the state of all queued tasks and may order the execution of any task, marked as “ready for execution”, by sending a command indicating its task ID. The device executes the data transfer transaction after receiving the execute command (CMD46/CMD47)

CMD Set Description

Table 4-5 CMD Set Description and Details

CMD	Type	Argument	Abbreviation	Purpose
CMD44	ac/R1	[31] Reliable Write Request [30] DAT_DIR - "0" write / "1" read [29] tag request [28:25] context ID [24] forced programming [23] Priority: “0” simple / “1” high [20:16] TASK ID [15:0] number of blocks	QUEUED_TASK _PARAMS	Define direction of operation (Read or Write) and Set high priority CMD Queue with task ID
CMD45	ac/R1	[31:0] Start block address	QUEUED_TASK_ADDRESS	Indicate data address for Queued CMD
CMD46	adtc/R1	[20:16] TASK ID	EXECUTE_READ_TASK	(Read) Transmit the requested number of data
CMD47	adtc/R1	[20:16] TASK ID	EXECUTE_WRITE_TASK	(Write) Transmit the requested number of data
CMD48	ac/R1b	[20:16] Task ID [3:0] TM op-code	CMDQ_TASK _MGMT	Reset a specific task or entire queue. [20:16] when TM op-code = 2h these bits represent TaskID.

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New Response: QSR (Queue Status Register)

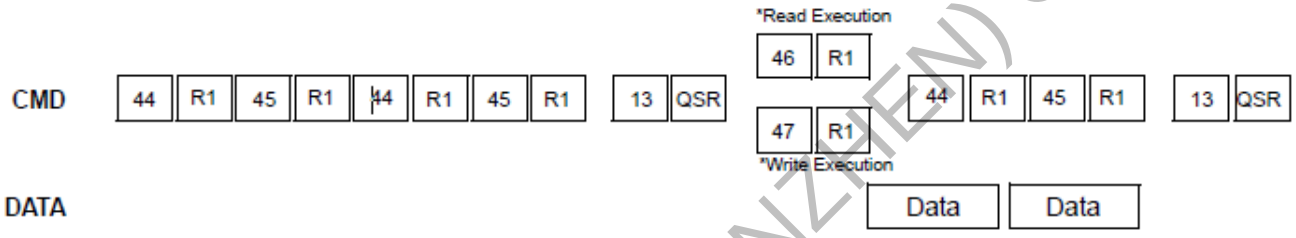
The 32-bit Queue Status Register (QSR) carries the state of tasks in the queue at a specific point in time. The host has read access to this register through device response to SEND_STATUS command (CMD13 with bit[15]="1"), R1's argument will be the 32-bit Queue Status Register (QSR). Every bit in the QSR represents the task who's ID corresponds to the bit index. If bit QSR[i] = "0", then the queued task with a Task ID i is not ready for execution. The task may be queued and pending, or the Task ID is unused. If bit QSR[i] = "1", then the queued task with Task ID i is ready for execution.

Send Status: CMD13

CMD13 for reading the Queue Status Register (QSR) by the host. If bit[15] in CMD13's argument is set to 1, then the device shall send an R1 Response with the QSR instead of the Device Status. * There is still legacy CMD13 with R` response.

Mechanism of CMD Queue operation

Host issues CMD44 with Task ID number, Sector, Count, Direction, Priority to the device followed by CMD45 and host checks the Queue Status check with CMD13 [15]bits to 1 . After that host issues CMD46 for Read or CMD47 for write During CMD queue operation, CMD44/CMD45 is able to be issued at anytime when the CMD line is not in use



CMD Queue Register description

Configuration and capability structures shall be added to the EXT_CSD register, as described below

Table 4-6 CMD Queuing Support (EXT_CSD register: CMDQ_SUPPORT [308])

Bit7	Bit6	Bit5	Bit4	Bit 3	Bit2	Bit1	Bit0
Reserved							CMD Queue supportability

This field indicates whether the device supports command queuing or not
0x0: CMD Queue function is not supported
0x1: CMD Queue function is supported

Table 4-7 Command Queue Mode Enable (EXT_CSD register: CMDQ_MODE_EN [15])

Bit7	Bit6	Bit5	Bit4	Bit 3	Bit2	Bit1	Bit0
Reserved							0x00

This field is used by the host enable command queuing
0x0: Queue function is not enabled
0x1: Queue function is enabled

Table 4-8 CMD Queuing Depth (EXT_CSD register: CMDQ_DEPTH [307])

Bit7	Bit6	Bit5	Bit4	Bit 3	Bit2	Bit1	Bit0
Reserved			0x0F				

This field is used to calculate the depth of the queue supported by the device
Bit encoding:
[7:5]: Reserved
[4:0]: N,a parameter used to calculate the Queue Depth of task queue in the device.
Queue Depth = N+1.

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6.3 Enhanced Strobe Mode

This product supports Enhanced Strobe in HS400 mode and refers to the details as described in eMMC5.1 JEDEC standard

6.4 RPMB Throughput improve

Table 4-9 Relate parameter register in EXT_CSD: WR_REL_PARAM [166]

Name	Field	Bit	Type
Enhanced RPMB Reliable Write	EN_RPMB_REL_WR	4	R

Bit [4]: EN_RPMB_REL_WR(R)

0x0: RPMB transfer size is either 256B (single 512B frame) or 512B (Two 512B frame).

0 x1: RPMB transfer size is either 256B (single 512B frame), 512B (Two 512B frame), or 8KB (Thirthy two 512B frames).

6.5 Secure Write Protection

Configuration and capability structures shall be added to the EXT_CSD register and Authenticated Device Configuration Area as described below

Table 4-10 Parameter register in EXT_CSD: SECURE_WP_INFO [211]

Bit7	Bit6	Bit5	Bit4	Bit	Bit2	Bit1	Bit0
Reserved						SECURE_WP_EN_STAT	SECURE_WP_SUPPOR

Bit [7:2]: Reserved

Bit [1]: SECURE_WP_EN_STATUS(R)

0x0: Legacy Write Protection mode.

0x1: Secure Write Protection mode.

Bit [0]: SECURE_WP_SUPPORT(R)

0x0: Secure Write Protection is NOT supported by this device

0x1: Secure Write Protection is supported by this device

Table 4-11 Authenticated Device Configuration Area [1]: SECURE_WP_MODE_ENABLE

Bit7	Bit6	Bit5	Bit4	Bit	Bit2	Bit1	Bit0
Reserved							0x00

Bit [7:1]: Reserved

Bit [0]: SECURE_WP_EN (R/W/E)

The default value of this field is 0x0.

- 0x0: Legacy Write Protection mode, i.e., TMP_WRITE_PROTECT[12] , PERM_WRITE_PROTECT[13] is updated by CMD27. USER_WP[171], BOOT_WP[173] and BOOT_WP_STATUS[174] are updated by CMD6.
- 0x1: Secure Write Protection mode. The access to the write protection related EXT_CSD and CSD fields depends on the value of SECURE_WP_MASK bit in SECURE_WP_MODE_CONFIG field.

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Table 4-12 Authenticated Device Configuration Area[2]: SECURE_WP_MODE_CONFIG

Bit7	Bit6	Bit5	Bit4	Bit	Bit2	Bit1	Bit0
Reserved							0x00

Bit [7:1]: Reserved
Bit [0]: SECURE_WP_MASK (R/W/E_P)
The default value of this field is 0x0.

- 0x0: Disabling updating WP related EXT_CSD and CSD fields. CMD27 (Program CSD) will generate generic error for setting TMP_WRITE_PROTECT[12], PERM_WRITE_PROTECT[13]. CMD6 for updating USER_WP[171], BOOT_WP[173] and BOOT_WP_STATUS[174] generates SWITCH_ERROR. If a force erase command is issued, the command will fail (Device stays locked) and the LOCK_UNLOCK_FAILED error bit will be set in the status register. If CMD28 or CMD29 is issued, then generic error will be occurred.

  Power-on Write Protected boot partitions will keep protected mode after power failure, H/W reset assertion and any CMD0 reset. The device keeps the current value of BOOT_WP_STATUS in the EXT_CSD register to be same after power cycle, H/W reset assertion, and any CMD0 reset.

- 0x1: Enabling updating WP related EXT_CSD and CSD fileds. I.e TMP_WRITE_PROTECT[12], PERM_WRITE_PROTECT[13], USER_WP[171], BOOT_WP[173] and BOOT_WP_STATUS[174] are accessed using CMD6, CMD8 and CMD27.

  If a force erase command is issued and accepted, then ALL THE DEVICE CONTENT WILL BE ERASED including the PWD and PWD_LEN register content and the locked Device will get unlocked. If a force erase command is issued and power-on protected or a permanently-writeprotected write protect groups exist on the device, the command will fail (Device stays locked) and the LOCK_UNLOCK_FAILED error bit will be set in the status register. An attempt to force erase on an unlocked Device will fail and LOCK_UNLOCK_FAILED error bit will be set in the status register. Write Protection is applied to the WPG indicated by CMD28 with the WP type indicated by the bit[2] and bit[0] of USER_WP[171]. All temporary WP Groups and power-on Write Protected boot partitions become writable/erasable temporarily which means write protect type is not changed. All power-on and permanent WP Groups in user area will not become writable/erasable temporarily. Those temporarily writable/erasable area will become write protected when this bit is cleared to 0x0 by the host or when there is power failure, H/W reset assertion and any CMD0 reset. The device keeps the current value of BOOT_WP_STATUS in the EXT_CSD register to be same after power cycle, H/W reset assertion, and any CMD0 reset.

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6.6 Technical Notes

S/W Algorithm

Partition Management

The device initially consists of two Boot Partitions and RPMB Partition and User Data Area.

The User Data Area can be divided into four General Purpose Area Partitions and User Data Area partition. Each of the General Purpose Area partitions and a section of User Data Area partition can be configured as enhanced partition.

Enhanced Partition (Area)

eMMC adopts Enhanced User Data Area as SLC Mode. Therefore when master adopts some portion as enhanced user data area in User Data Area, that area occupies double size of original set up size. (ex> if master set 1MB for enhanced mode, total 2MB user data area is needed to gen- erate 1MB enhanced area)

Max Enhanced User Data Area size is defined as (MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512Kbytes)

Boot operation

Device supports not only boot mode but also alternative boot mode. Device supports high speed timing and dual data rate during boot.

Figure 4-1 embedded MultiMediaCard state diagram (boot mode)

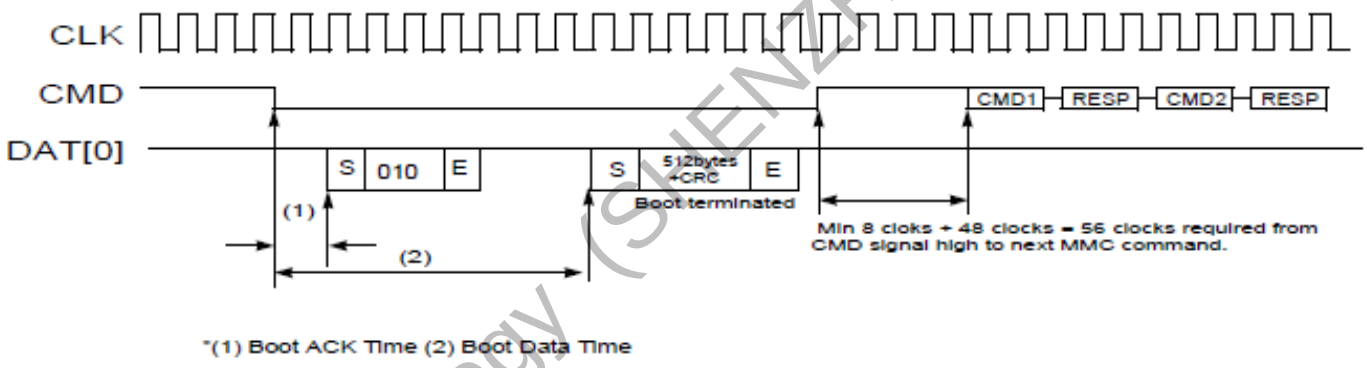
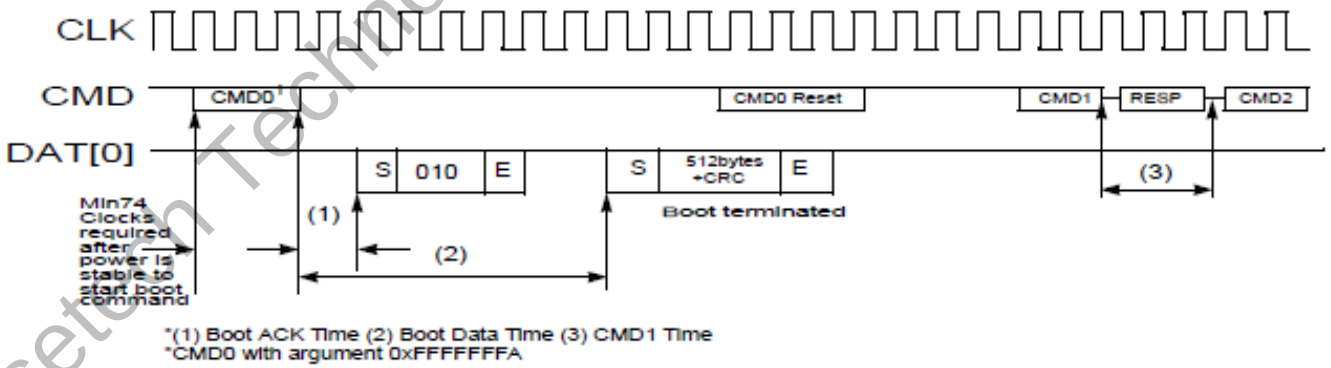


Figure 4-2 embedded MultiMediaCard state diagram (alternative boot mode)



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Table 4-13 Boot ack, boot data and initialization Time

Timing Factor	Value
Boot ACK Time	< 50 ms
Boot Data Time	< 100 ms
Initialization Time[1]	< 3 secs

Note:

1. This initialization time includes partition setting, Please refer to INI_TIMEOUT_AP in Extended CSD Register. Normal initialization time (without partition setting) is completed within 1sec

User Density

Total User Density depends on device type.
For example, 32MB in the SLC Mode requires 64MB in MLC.
This results in decreasing of user density

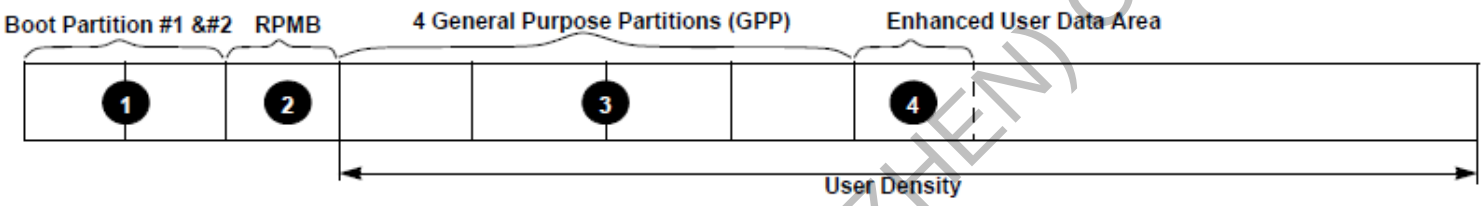


Table 4-14 Capacity according to partition

Device	Boot partition 1 [KB]	Boot partition 2 [KB]	RPMB[KB]
32GB	4,096	4,096	4,096

Table 4-15 User Density Size

Device	User Partition Size
32GB	31,272,730,624 Bytes

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Auto Power Saving Mode

If host does not issue any command during a certain duration (1ms), after previously issued command is completed, the device enters "Power Saving mode" to reduce power consumption.

At this time, commands arriving at the device while it is in power saving mode will be serviced in normal fashion

Table 4-16 Auto Power Saving Mode enter and exit

Mode	Enter Condition	Escape Condition
Auto Power Saving Mode	When previous operation which came from Host is completed and no com-mand is issued during a certain time.	If Host issues any command

Table 4-17 Auto Power Saving Mode and Sleep Mode

Mode	Enter Condition	Escape Condition
NAND Power	ON	OFF
GotoSleep Time	< 1ms	< 1ms

Performance

Table 4-18 Sustained Sequential Performance

Density (GB)	Sequential Read (MB/s)	Sequential Write (MB/s)
32	330	100

Note:

1. Test Condition: Bus width x8, HS400, 512KB data transfer, Packed Off, Cache On, w/o file system overhead.

6.7 Register Value

OCR Register

The 32-bit operation conditions register stores the VCCQ voltage profile of the eMMC. In addition, this register includes a status information bit. This status bit is set if the eMMC power up procedure has been finished. The OCR register shall be implemented by all eMMCs.

Table 4-19 OCR Register

OCR bit	V_{CCQ} Voltage Window[2]	Register Value
[6:0]	Reserved	00 00000b
[7]	1.70 ~ 1.95	1b
[14:8]	2.0 ~ 2.6	000 0000b
[23:15]	2.7 ~ 3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	00b (byte mode) 10b (sector mode) -[*Higher than 2GB only]
[31]	eMMC power up status bit (busy)[1]	

Notes:

1. This bit is set to LOW if the eMMC has not finished the power up routine.
2. The voltage for internal flash memory (V_{CC}) should be 2.7 ~ 3.6V regardless of OCR register value.

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CID Register

Table 4-20 CID Register

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	0xAD
Reserved		6	[119:114]	–
Card/BGA	CBX	2	[113:112]	01
OEM/Application ID	OID	8	[111:104]	–
Product name	PNM	48	[103:56]	–
Product revision	PRV	8	[55:48]	–
Product serial number	PSN	32	[47:16]	–
Manufacturing date	MDT	8	[15:8]	–
CRC7 checksum	CRC	7	[7:1]	–
not used, always '1'	–	1	[0:0]	–

Notes:

1. Tdescription are same as eMMC JEDEC standard.
2. PRV is composed of the revision count of controller and the revision count of F/W patch.
3. A 32 bits unsigned binary integer. (Random Number).

CSD Register

The Card-Specific Data register provides information on how to access the eMMC contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27.

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Table 4-22 CSD Register

Name	Field	Bit	Type	Slice	Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x03
System specification version	SPEC_VERS	4	R	[125:122]	0x04
Reserved	–	2	R	[121:120]	–
Data read access-time 1	TAAC	8	R	[119:112]	0x27
Data read access-time 2 in CLK cycles (NSAC x 100)	NSAC	8	R	[111:104]	0x01
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x32
Device command classes	CCC	12	R	[95:84]	0xF5
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x09
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x00
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x00
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x00
DSR implemented	DSR_IMP	1	R	[76:76]	0x00
Reserved	–	2	R	[75:74]	–
Device size	C_SIZE	12	R	[73:62]	0xFFF
Max read current@VCCQ min	VCCQ_R_CURR_MIN	3	R	[61:59]	0x06
Max read current@VCCQ max	VCCQ_R_CURR_MAX	3	R	[58:56]	0x06
Max write current@VCCQ min	VCCQ_W_CURR_MIN	3	R	[55:53]	0x06
Max write current@VCCQ max	VCCQ_W_CURR_MAX	3	R	[52:50]	0x06
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	0x07
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0x0F
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	0x01
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0x00
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x03
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x09
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x00
Reserved	–	4	R	[20:17]	–
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0x00
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0x00
Copy flag (OTP)	COPY	1	R/W	[14:14]	0x01
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x00

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Table 4-22 CSD Register (Continued)

Name	Field	Bit	Type	Slice	Value
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x00
File format	FILE_FORMAT	2	R/W	[11:10]	0x00
ECC code	ECC	2	R/W/E	[9:8]	0x00
CRC	CRC	7	R/W/E	[7:1]	–
Not used, always '1'	–	1		[0:0]	–

Note:

1. The type of the CSD Registry entries in the Table 4-22 is coded as follows.
   R: Read only
   W: One time programmable and not readable
   R/W: One time programmable and readable
   W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
   R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
   R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
   R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
   W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

Extended CSD Register

The Extended CSD register defines the eMMC properties and selected modes. It is 512 bytes long.

The most significant 320 bytes are the Properties segment, which defines the eMMC capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the eMMC is working in. These modes can be changed by the host by means of the SWITCH command.

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Table 4-23 Typical EXT_CSD Register

Name	Field	Byte	Type	Slice	Value
Properties Segment					
Reserved		6	–	[511:506]	–
Extended security commands error	EXT_SECURITY_ERR	1	R	[505]	0x00
Supported command sets	S_CMD_SET	1	R	[504]	0x01
HPI features	HPI_FEATURES	1	R	[503]	0x01
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x01
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x3F
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x3F
Data tag support	DATA_TAG_SUPPORT	1	R	[499]	0x01
Tag unit size	TAG_UNIT_SIZE	1	R	[498]	0x02
Tag resources size	TAG_RES_SIZE	1	R	[497]	0x00
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x05
Large unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x07
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	0x03
Supported modes	SUPPORTED_MODES	1	R	[493]	0x03
FFU features	FFU_FEATURES	1	R	[492]	0x00
Operation codes timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	0x00
FFU Argument	FFU_ARG	4	R	[490:487]	0xC7810000
Barrier Support	BARRIER_SUPPORT	1	R	[486]	0x00
Reserved		177	–	[485:309]	–
CMD Queuing Support	CMDQ_SUPPORT	1	R	[308]	0x01
CMD Queuing Depth	CMDQ_DEPTH	1	R	[307]	0x0F
Reserved		1	–	[306]	–
Number of FW sectors correctly programmed	NUMBER_OF_FW_ SECTOR S_CORRECTLY_ PROGRAM MED	4	R	[305:302]	0x01
Vendor proprietary health report	VENDOR_PROPRIETARY_ HEALTH_REPORT	32	R	[301:270]	0x01
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	0x01
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	0x00

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Table 4-23 Typical EXT_CSD Register (Continued)

Name	Field	Byte	Type	Slice	Value
Properties Segment					
Pre EOL information	PRE_EOL_INFO	1	R	[267]	0x10
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x01
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x00
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x01
Device version	DEVICE_VERSION	1	R	[263:262]	0x00
Firmware version	FIRMWARE_VERSION	3	R	[261:254]	0x01
Power class for 200MHz, DDR at 3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x00
Cache size	CACHE_SIZE	4	R	[252:249]	0x10000
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x0A
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x3C
Background operations status	BKOPS_STATUS	1	R	[246]	0x00
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x00
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x1E
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	[240]	–
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x00
Power class for 52 MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x00
Power class for 200MHz at VCCQ=1.95V, VCC=3.6V	PWR_CL_200_360	1	R	[237]	0x00
Power class for 200MHz, at VCCQ=1.3V, VCC=3.6V	PWR_CL_200_195	1	R	[236]	0x00
Minimum write performance for 8 bit at 52 MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x00
Minimum read performance for 8 bit at 52 MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x00
Reserved		1	–	[233]	–
TRIM multiplier	TRIM_MULT	1	R	[232]	0x02
Secure feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55
Secure erase multiplier	SEC_ERASE_MULT	1	R	[230]	0x1B
Secure trim multiplier	SEC_TRIM_MULT	1	R	[229]	0x11
Boot information	BOOT_INFO	1	R	[228]	0x07
Reserved		1	–	[227]	–
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	0x20

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Table 4-23 Typical EXT_CSD Register (Continued)

Name	Field	Byte	Type	Slice	Value
Properties Segment					
Access size	ACC_SIZE	1	R	[225]	0x07
High-capacity erase unit siz	HC_ERASE_GRP_SIZE	1	R	[224]	0x01
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x01
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x01
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x10
Sleep current (V_{CC})	S_C_VCC	1	R	[220]	0x07
Sleep current (V_{CCQ})	S_C_VCCQ	1	R	[219]	0x07
Product state awareness timeout	PRODUCTION_STATE_ AWARENESS_TIMEOUT	1	R	[218]	0x00
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x11
Sleep notification timeout	SLEEP_NOTIFICATION_TIME	1	R	[216]	0x07
Sector count	SEC_COUNT	4	R	[215:212]	0x3A4E000
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	0x01
Minimum write performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	[210]	0x00
Minimum read performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	0x00
Minimum write performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x00
Minimum read performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x00
Minimum write performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	0x00
Minimum read performance for 4bit at 26MHz	MIN_PERFR_4_26	1	R	[205]	0x00
Reserved		1	–	[204]	–
Power class or 26 MHz at 3.6V 1 R	PWR_CL_26_360	1	R	[203]	0x00
Power class for 52 MHz at 3.6V 1 R	PWR_CL_52_360	1	R	[202]	0x00
Power class for 26 MHz at 1.95V 1 R	PWR_CL_26_195	1	R	[201]	0x00
Power class for 52 MHz at 1.95V 1 R	PWR_CL_52_195	1	R	[200]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x02
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x0A

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Table 4-23 Typical EXT_CSD Register (Continued)

Name	Field	Byte	Type	Slice	Value
Properties Segment					
I/O Driver Strength CSD structure version	DRIVER_STRENGTH	1	R	[197]	0x1F
Device type	DEVICE_TYPE	1	R	[196]	0x57
Reserved		1	–	[195]	–
CSD structure version	CSD_STRUCTURE	1	R	[194]	0x02
Reserved		1	–	[193]	–
Extended CSD revision	EXT_CSD_REV	1	R	[192]	0x08
Modes Segment					
Command set	CMD_SET	1	R/W/E_P	[191]	0x00
Reserved		1	–	[190]	–
Command set revision	CMD_SET_REV	1	R	[189]	0x00
Reserved		1	–	[188]	–
Power class	POWER_CLASS	1	R/W/E_P	[187]	0x00
Reserved		1	–	[186]	–
High speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0x00
Strobe Support	STROBE_SUPPORT -	1	R	[184]	0x01
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0x00
Reserved		1	–	[182]	–
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0x00
Reserved		1	–	[180]	–
Partition configuration	PARTITION_CONFI	1	R/W/E & R/W/E_P	[179]	0x00
Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/C_P	[178]	0x00
Boot bus conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x0
Reserved		1	–	[176]	–
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0x00
Boot write protection status registers	BOOT_WP_STATU	1	R	[174]	0x00
Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	[173]	0x00
Reserved		1	–	[172]	–
User area write protection register	USER_WP	1	R/W, R/W/C_P & R/W/E_P	[171]	0x00

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Table 4-23 Typical EXT_CSD Register (Continued)

Name	Field	Byte	Type	Slice	Value
Reserved		1	–	[170]	–
FW configuration	FW_CONFIG	1	R/W	[169]	0x00
RPMB size	RPMB_SIZE_MULT	1	R	[168]	0x20
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x14
Start sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x00
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	0x00
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x00
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x00
Partitioning support	PARTITIONING_SUPPORT	1	R	[160]	0x07
Max enhanced area size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0x748
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x00
Partitioning setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	0x00
General purpose partition size	GP_SIZE_MULT	12	R/W	[154:143]	0x00
Enhanced user data area size	ENH_SIZE_MULT	3	R/W	[142:140]	0x00
Enhanced user data start address	ENH-START_ADDR	4	R/W	[139:136]	0x00
Reserved		1	–	[135]	–
Bad block management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x00
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	0x00
Package case temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x00
Periodic wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x00
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_ SUPPORT	1	R	[130]	0x01
Reserved		2	–	[129:128]	–
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	<vendor specific>	[127:64]	–
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x00
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x00
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x00
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x00

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Table 4-23 Typical EXT_CSD Register (Continued)

Name	Field	Byte	Type	Slice	Value
Modes Segment					
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x00
Number of addressed group to be released	DYNCAP_NEEDED	1	R	[58]	0x00
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x00
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0x00
Extended partitions attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0x00
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x00
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0x00
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x00
Power off notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x00
Control to turn the cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0x00
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x00
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R	[31]	0x00
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0x00
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0x00
Reserved		2	–	[28:27]	–
FFU status	FFU_STATUS	1	R	[26]	0x00
Pre loading data size	PRE_LOADING_ DATA_SIZE	4	R/W/E_P	[25:22]	0x00
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	0x00
Product state awareness enablement	PRODUCT_STATE_ AWARENESS_ ENABLEMENT	1	R/W/E & R	[17]	0x00
Secure removal type	SECURE_REMOVAL_TYPE	1	R/W/E & R	[16]	0x39
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0x00
Reserved		15	–	[14:0]	–

Note:

1. Reserved bits should be read as “0.”
2. The following is for the type of the EXT_CSD Register entries.
   R: Read only.
   W: One time programmable and not readable.
   R/W: One time programmable and readable.
   W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
   R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
   R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
   R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
   W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

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6.8 AC Parameter

Timing Parameter

Table 4-24 Timing Parameters

Timing Paramter		Max. Value
Initialization Time (tINIT)	Normal [1]	1 sec
	After partition setting [2]	3 sec
Read Timeout		100 ms
Write Timeout		350 ms
Erase Timeout		20 ms
Force Erase Timeout		3 min
Secure Erase Timeout		8 sec
Secure Trim step1 Timeout		5 sec
Secure Trim step2 Timeout		3 sec
Trim Timeout		600 ms
Partition Switching Timeout (after Init)		1 ms
Power Off Notification (Short) Timeout		100 ms
Power Off Notification (Long) Timeout		600 ms

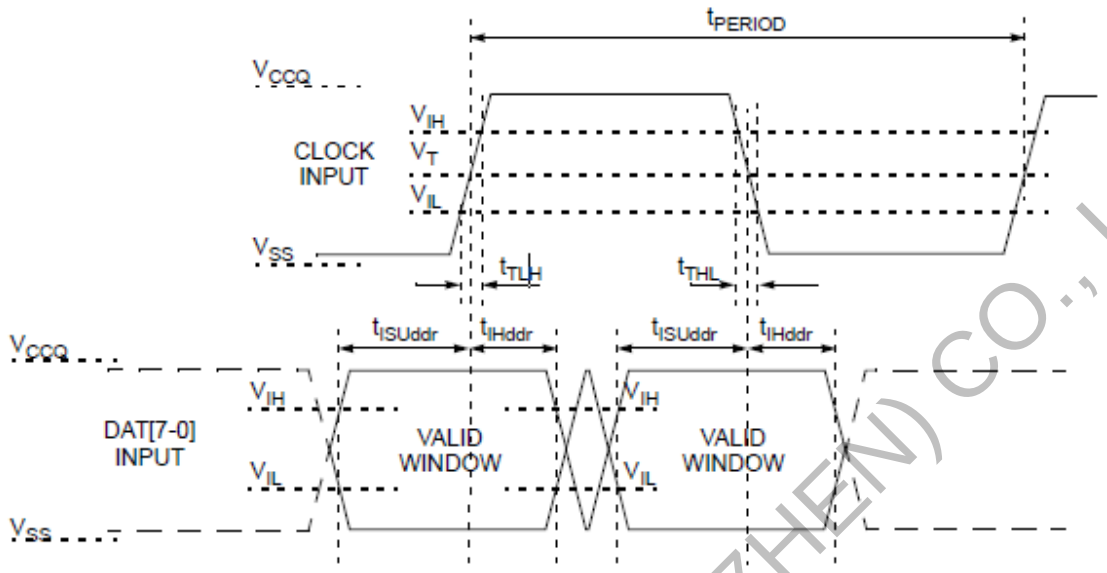
Notes:

1. Normal Initialization Time without partition setting
2. Initialization Time after partition setting, refer to INI_TIMEOUT_AP in EXT_CSD register
3. Be advised Timeout Values specified in Table above are for testing purposes under test pattern only and actual timeout situations may vary
4. EXCEPTION_EVENT may occur and the actual timeout values may vary due to user environment

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Bus Timing Specification in HS400 mode
HS400 Device Input Timing

Figure 4-3 HS400 Device Input Timing



Notes:

1. t_{ISU} and t_{IH} are measured at $V_{IL\ (max)}$ and $V_{IH\ (min)}$.
2. V_{IH} denotes $V_{IH\ (min)}$ and V_{IL} denotes $V_{IL\ (max)}$.

Table 4-25 HS400 Device Input Timing

Parameter	Symbol	Min	Max	Unit
Input CLK				
Cycle time data transfer mode	tPERIOD	5		ns
Slew rate	SR	1.125		V/ns
Duty cycle distortion	tCKDCD	0.0	0.3	ns
Minimum pulse width	tCKMPW	2.2		ns
Input DAT (referenced to CLK)				
Input set-up time	tISUddr	0.4		ns
Input hold time	tIHddr	0.4		ns
Slew rate	SR	1.125		V/ns

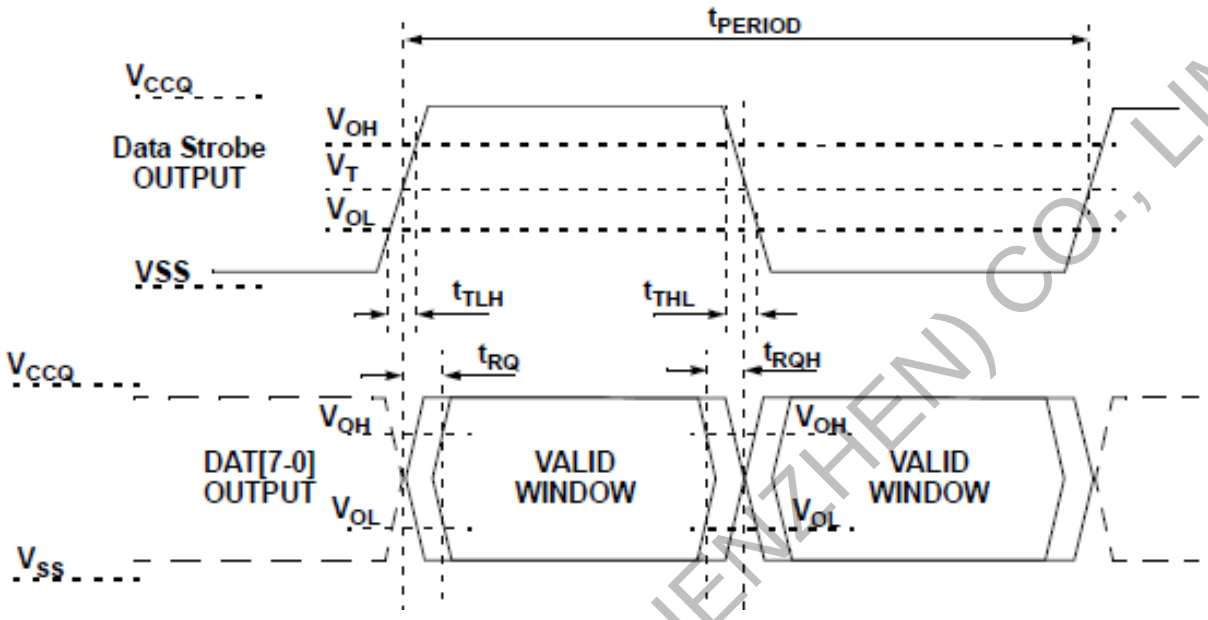
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HS400 Device Onput Timing

Data Strobe is used to read data (data read and CRC status response read) in HS400 mode.

The device output value of Data Strobe is “High-Z” when the device is not in outputting data (data read, CRC status response). Data Strobe is toggled only during data read period.

Figure 4-4 HS400 Device Output Timing Diagram



Note:

1. V_{OH} denotes $V_{OH\ (min)}$ and V_{OL} denotes $V_{OL\ (max)}$.

Table 4-26 HS400 DeviceOutput Timing

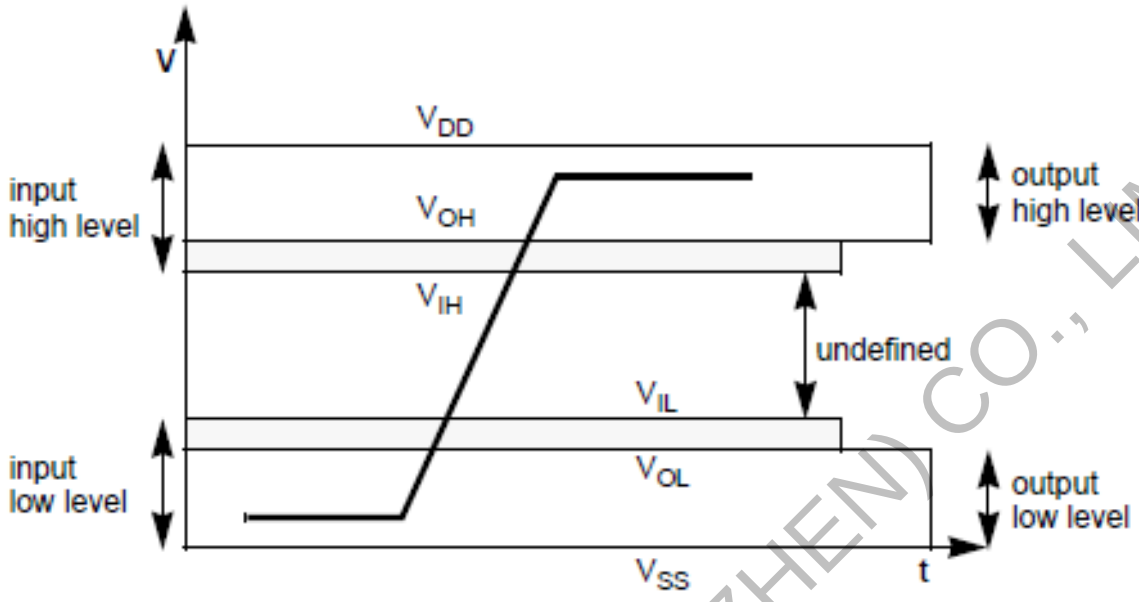
Parameter	Symbol	Min	Max	Unit
Data Strobe				
Cycle time data transfer mode	tPERIOD	5		ns
Slew rate	SR	1.125		V/ns
Duty cycle distortion	tDSDCD	0.0	0.2	ns
Minimum pulse width	tDSMPW	2.0		ns
Read pre-amble	tRPRE	0.4	-	tPERIOD
Read post-amble	tRPST	0.4	-	tPERIOD
Output DAT (referenced to Data Strobe)				
Output skew	tRQ	-	0.4	ns
Output hold skew	tRQH	-	0.4	ns
Slew rate	SR	1.125		V/ns

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Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

Figure 4-5 Bus Signal Levels



Open-drain mode bus Signal Levels

Table 4-27 Open-drain bus signal Level

Paramter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{DD} – 0.2	–	V	
Output LOW voltage	V_{OL}	–	0.3	V	I_{OL} = 2 mA

Note:

1. Because Voh depends on external resistance value (including outside the package), this value does not apply as device specification.
   Host is responsible to choose the external pull-up and open drain resistance value to meet Voh Min value.

Push-pull mode bus signal level eMMC

The device input and output voltages shall be within the following specified ranges for any VCCQ of the allowed voltage range

Table 4-28 Push-pull signal level — high-voltage eMMC

Paramter	Symbol	Min	Max	Unit	Remark
Output HIGH voltage	V_{OH}	0.75 x V_{DD}	–	V	I_{OH} = –100uA @ V_{CCQ} min
Output LOW voltage	V_{OL}	–	0.125 x V_{DD}	V	I_{OL} = 100uA @ V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625 x V_{DD}	V_{DD} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.3	0.25 x V_{DD}	V	

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Table 4-29 Push-pull signal level — 1.70 - 1.95 VCCQ voltage Range

Paramter	Symbol	Min	Max	Unit	Remark
Output HIGH voltage	V_{OH}	V_{CCQ} – 0.45V	–	V	I_{OH} = -2mA
Output LOW voltage	V_{OL}	–	0.45V	V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65 x V_{CCQ}	V_{CCQ} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.3	0.35 x V_{CCQ}	V	

Notes:
1. 0.7*VCCQ for MMC4.3 and older revisions.
2. 0.3*VCCQ for MMC4.3 and older revisions.

6.9 DC Parameter

Power Consumption

Table 4-30 Active Power Consumption during operation

Density (GB)	NAND Type	VCCQ (Max RMSmA)	Vcc (Max RMS,mA)
32	256Gb x 1	180	100

Notes:
1. Power Measurement conditions: Bus configuration =x8 @HS400.
6. The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

Table 4-31 Standby Power Consumption in auto power saving mode and standby state

Density (GB)	NAND Type	VCCQ (uA)		Vcc (uA)	
		25°C (Typ)	85°C	25°C (Typ)	85°C
32	256Gb x1	120	400	50	135

Notes:
1. Power Measurement conditions: Bus configuration =x8, No CLK.
2. Typical value is measured at V_{CC}/V_{CCQ}=3.3V, TA=25°C. Not 100% tested.

Table 4-32 Sleep Power Consumption in Sleep State

Density (GB)	NAND Type (MLC)	VCCQ (uA)		Vcc (uA)
		25°C (Typ)	85°C	
32	256Gb x 1	120	400	0

Notes:
1. Power Measurement conditions: Bus configuration =x8, No CLK.
2. In auto power saving mode, VCC power can not be turned off. However in sleep mode VCC power can be turned off.

Supply Voltage

Table 4-33 Supply Voltage

Symbol	Min (V)	Max (V)
V_{CCQ}	1.7	1.95
	3.0	3.6
V_{CC}	2.7	3.6
V_{SS}	-0.5	0.5

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Bus Signal Line Load

The total capacitance CL of each line of the eMMC bus is the sum of the bus master capacitance CHOST, the bus capacitance CBUS itself and the capacitance CDEVICE of the eMMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

Table 4-34 Bus SIgnal Line Load

Paramter	Symbol	Min	Typ	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	KOhm	to prevent bus floating
Pull-up resistance for DAT0-DAT7	R_{DAT}	10		100	KOhm	to prevent bus floating
Internal pull up resistance DAT1-DAT7	R_{int}	10		150	KOhm	to prevent unconnected lines floating
Single Device capacitance	C_{DEVICE}			12	pF	
Maximum signal line inductance				16	nHV	f_{PP}<= 52 MHz

Table 4-35 Capacitance and Resistance for HS400 mode

Paramter	Symbol	Min	Typ	Max	Unit	Remark
Bus signal line capacitance	C_L			13	pF	Single Device
Single Device capacitance	C_{DEVICE}			6	pF	
Pull-down resistance for Data Strobe	$R_{Data\ Strobe}$	10		100	KOhm	

6.10 Power Delivery And Capacitor Specifications

Power Domains

32GB eMMC has three power domains assigned to V_{CCQ}, V_{CC} and V_{DDI_M}, as shown below.

Table 4-36 Power Domains

Symbol	Power Domain	Comments
V_{CCQ}	Host Interface	
V_{CC}	Memory	
V_{DDI_M}	Internal	V_{DDI_M} is the internal regulator connection to an external decoupling capacitor.

Capacitor Connection Guidelines

It is recommended to place the following capacitors on V_{CC} & V_{CCQ} domains:

- C_1/C_3= 4.7uF
  - ◆ E.g.:

Manufacturer	Manufacturer P/N
MURATA	GRM185R60J475ME15D
TAIYO YUDEN	JMK107BJ475MK-T

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● C_2/C_4/C_6= 0.1uF

◆ E.g. :

Manufacturer	Manufacturer P/N
MURATA	GRM155R71A104KA01D
KYOCERA	CM05X5R104K06AH

For V_{CC} (3.3V), it is recommended to place:

● C_5 (V_{CC}) = 10uF

◆ E.g. :

Manufacturer	Manufacturer P/N
TAIYO YUDEN	JMK107ABJ106MAHT
PANASONIC	ECJ-1VB0J106M
SAMSUNG	CL10A106MQ8NNNC

Capacitors Type:
- SMT-Ceramic
- X5R
- 6.3V
- Min height – 0.55mm
- Foot Print: 0402 or above

Suggested capacitors should be located as close to the supply ball as possible and they will eliminate as much trace
inductance effects as possible and give cleaner voltage supply to device. Also, they reduce lead length and eliminate noise coupling onto through-hole components, which may have effects of antenna.

Make all of the power (high current) traces as short, direct, and thick as possible and put all capacitors as close to each other as possible, for reducing EMI radiated by the power traces due to the high switching currents through them. Again, it shall also reduce lead inductance and resistance as well and thus, noise spikes, ringings, and resistive losses which cause voltage errors.

For the ground of these capacitors, they should be connected close together directly to a ground plane and it is also recommended to have a ground plane on both sides of the PCB, to reduce noise by eliminating ground loop errors as well.

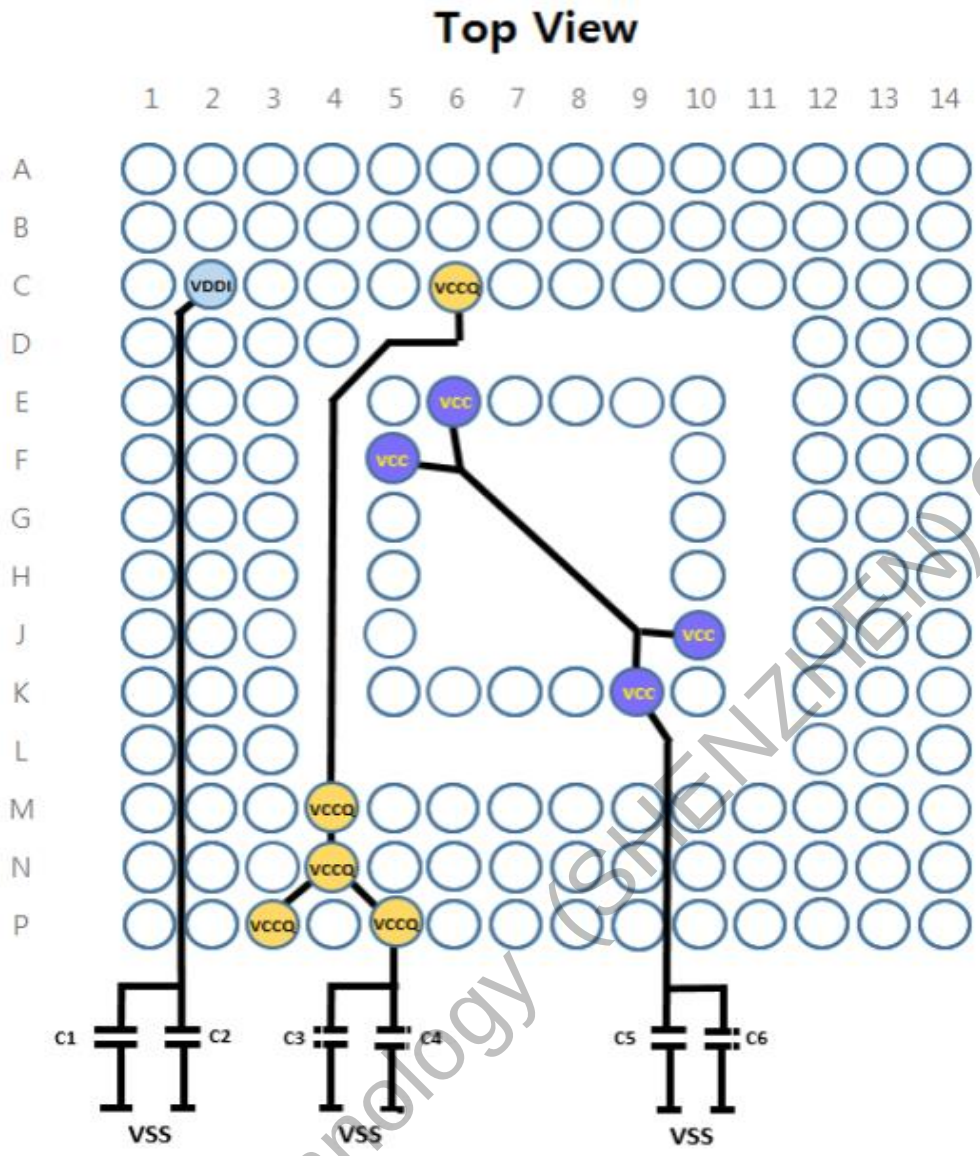
The loop inductance per capacitor shall not exceed 3nH (both on V_{CC}/V_{CCQ} & V_{SS} loops).

Multiple via connections are recommended per each capacitor pad.

Signal Traces:
- Data, CMD, CLK & RCLK bus trace length mismatch should be minimal (up to +/-1mm).
- Traces should be 50ohm controlled impedance.

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Figure 4-6 Recommended Power Domain Connections



Paramter	Symbol	Unit	Value
V_{DDI_M}	C1 + C2	uF	4.7 + 0.1
V_{CCQ}	C3 + C4	uF	4.7 + 0.1
V_{CC}	C5 + C6	uF	10 + 0.1

Note:
Coupling capacitor should be connected with V_{DD} and V_{SS} as closely as possible.

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