PLUSETECH DDR4 8GB 3200 UDIMM Datasheet

PSD4B08HA32UN-08G

Module Part Number	PSD4B08HA32UN-08G
Memory Type	DDR4
Module Type	Unbuffered UDIMM
Module Density	8GB
Data Width	x64
Data Rate	3200 MT/s
V_{DD} Voltage	1.2V
Interface	288-pin
Number of Ranks	2
SDRAM Device Width	x8
CAS Latency	CL22
Operation Temperature	0°C ~ +85°C
RoHS	Yes
Standard	JEDEC

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Features

- JEDEC Standard
- 288-pin, unbuffered dual in-line memory module(UDIMM)
- Fast data transfer rates: PC4-3200, backward compatible PC4-3000, PC4-2666, PC4-2400, PC4-2133
- 16GB (1G x 8 x 16PCS)
- V_{DD} = 1.2V (1.14-1.26V)
- Backward compatible to V_{DD} = 1.2V ± 0.06V
- V_{DDSPD} = 2.5V
- Nominal and dynamic on-die termination(ODT) for data, strobe, and mask signals
- Dual-rank
- 16 internal banks
- Bi-Directional Differential Data Strobe
- Programmable CAS latency 15, 16, 17, 18, 19, 20, 21, 22 supported
- On board I^2C with integrated serial presence-datect(SPD) EEPROM
- JEDEC standard 78ball FBGA(x8)
- Gold edge contacts
- This product in compliance with the RoHS directive
- Terminated control, command, and address bus

Options

- Operation temperature
  - Commercial 0°C ~ +85°C
- Package
  - 288-pin DIMM
- Frequency/CAS latency
  - 0.625ns @ CL = 22(DDR4-3200)

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Table 1: Key Timing Parameters

Part Number	Industrial Nomenclature	CAS Latency(CL)							
		22	21	20	19	18	17	16	15
PSD4B08HA32UN-08G	Pc4-3200	3200							
	PC4-3000		3000	3000					
	PC4-2666				2666	2666	2400	2133	2133
	PC4-2400					2400	2400	2133	2133
	PC4-2133							2133	2133

Table 2: Addressing

Parameter	16GB
Device Configuration	1Gb x 8bit x 16 pcs
ROW address	128K (A[14:0])
Column address	1K (A[9:0])
Device bank group address	4 (BG[1:0])
Device bank address per group	4 (BA[1:0])

Table 3: DDR4-3200 Speed Bins

Speed Bin		DDR4-3200		Unit	Note
CL - nRCD - nRP		22-22-22			
Parameter	Symbol	min	max		
Internal read command to first data	t_{AA}	13.75	19	ns	
ACT to internal read or write delay time	t_{RCD}	13.75	-	ns	
PRE command period	t_{RP}	13.75	-	ns	
ACT to ACT or REF command period	t_{RC}	45.75	-	ns	
ACT to PRE command period	t_{RAS}	32	9 * t_{REFI}	ns	

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Table 4: Operating Conditions

Recommended DC Operating Conditions – DDR4 (1.2V) operation

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.14	1.2	1.26	V	1,2,3
$V_{DD}Q$	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3

Notes:

1. Under all conditions, $V_{DD}Q$ must be less than or equal to V_{DD}.
2. $V_{DD}Q$ tracks with V_{DD}. AC parameters are measured with V_{DD} and $V_{DD}Q$ tied together.
3. Under these supply voltages, the device operates to this DDR4 specification.

Table 5: DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Normal Operating Temperature Range	0 to 85	℃	1,2

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85℃ under all operating conditions.

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Table 6：Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.4V~1.5V	V	1,3
$V_{DD}Q$	Voltage on $V_{DD}Q$ pin relative to V_{SS}	-0.4V~1.5V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4V~1.4V	V	1
T_{STG}	Storage Temperature	-55 to +100	℃	1,2

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

3. V_{DD} and $V_{DD}Q$ must be within 300mV of each other at all times, and V_{REF} must not be greater than 0.6*$V_{DD}Q$, When V_{DD} and $V_{DD}Q$ are less than 500mV; V_{REF} may be equal to or less than 300mV.

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PCB Feature overview

- **General**

  * Board size: 133.35 x 30.75 mm ±0.15 mm

  * Finished Board Thickness: 1.4 ±0.1 mm

* Panel: 5 pieces PCB per panel

*** 8-layer board**

  * Impedance: 40/50/55 Ohm ±10% (Single-ended)
    70/83/93 Ohm ±15% (Differential)

*** Pin count: 288 PIN**

- **PCB Material**

* Glass Epoxy FR4, .UL 94V-0, BP ML

- **Plating**

* Edge Connector Plating: Nickel Followed by gold

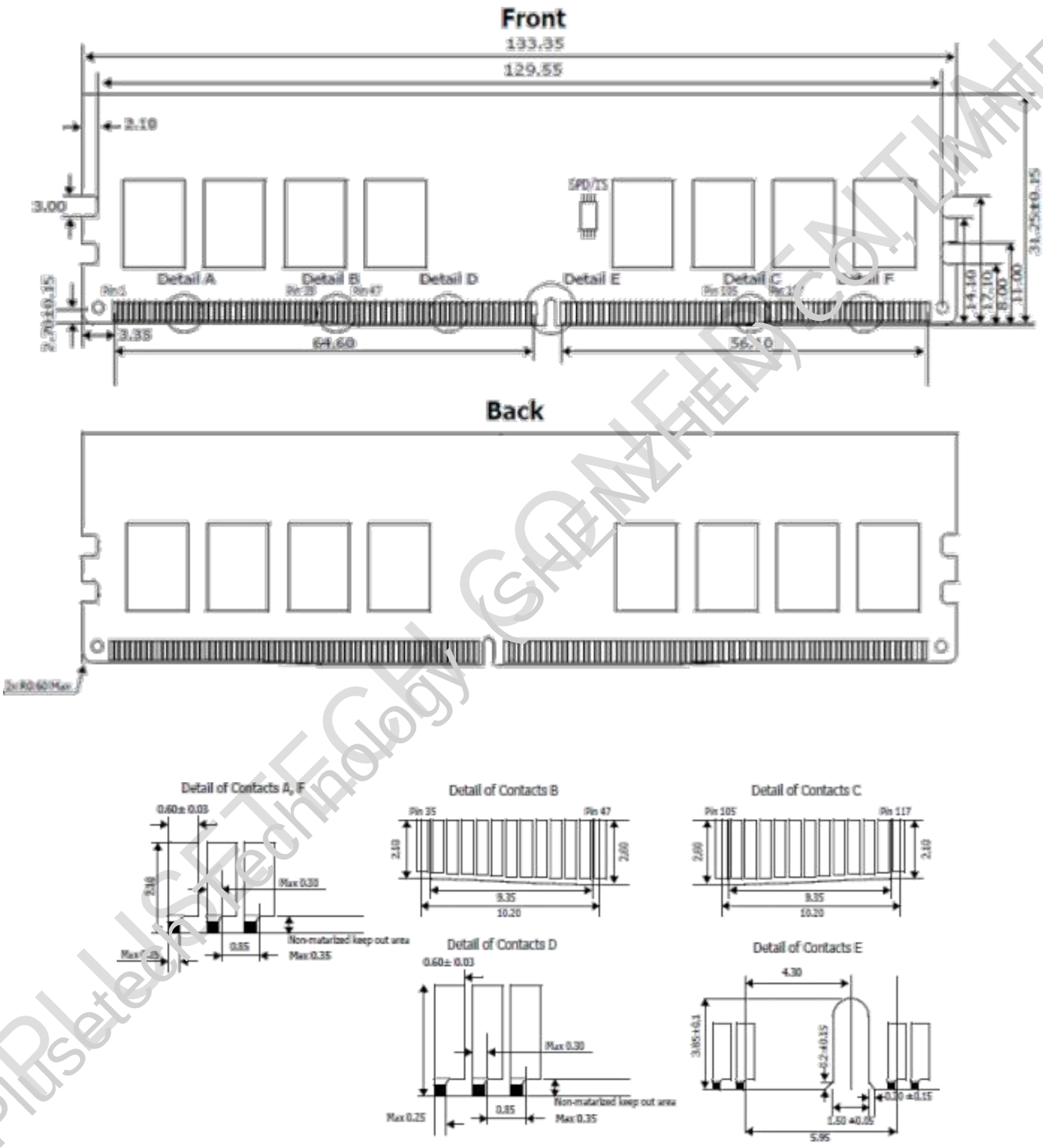
  - Nickel Plating Thickness: 100 u" min.
  - Surface treatment:
    Gold Plating: 3~5u" min.
    SMT PAD: average 2~3u".

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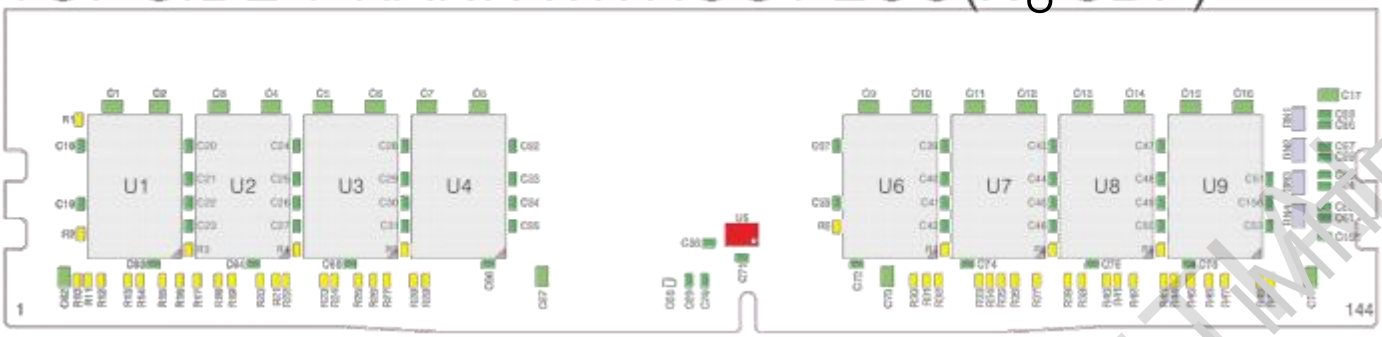
Module Dimensions

Figure 1: 288-pin DDR4 UDIMM

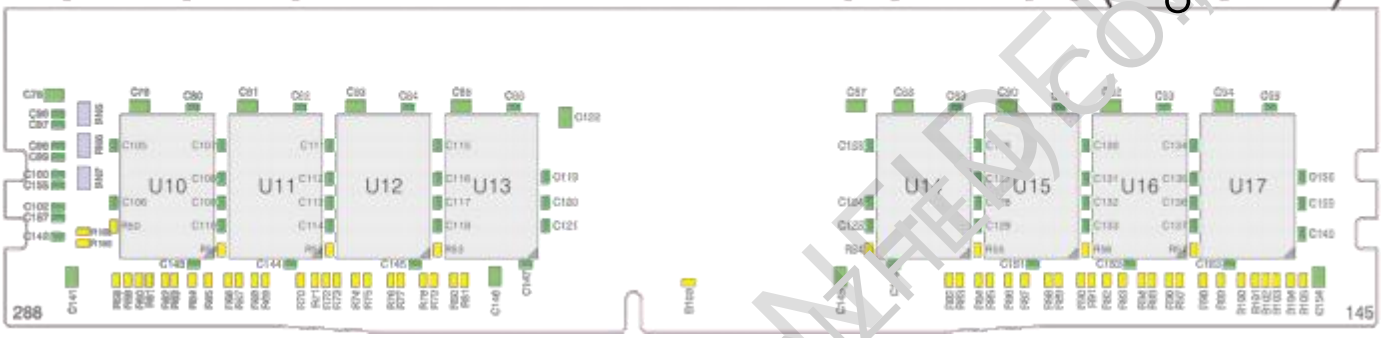


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TOP SIDE 1-RANK WITHOUT ECC(X8 SDP)



BOTTOM SIDE 1-RANK WITHOUT ECC(X8 SDP)

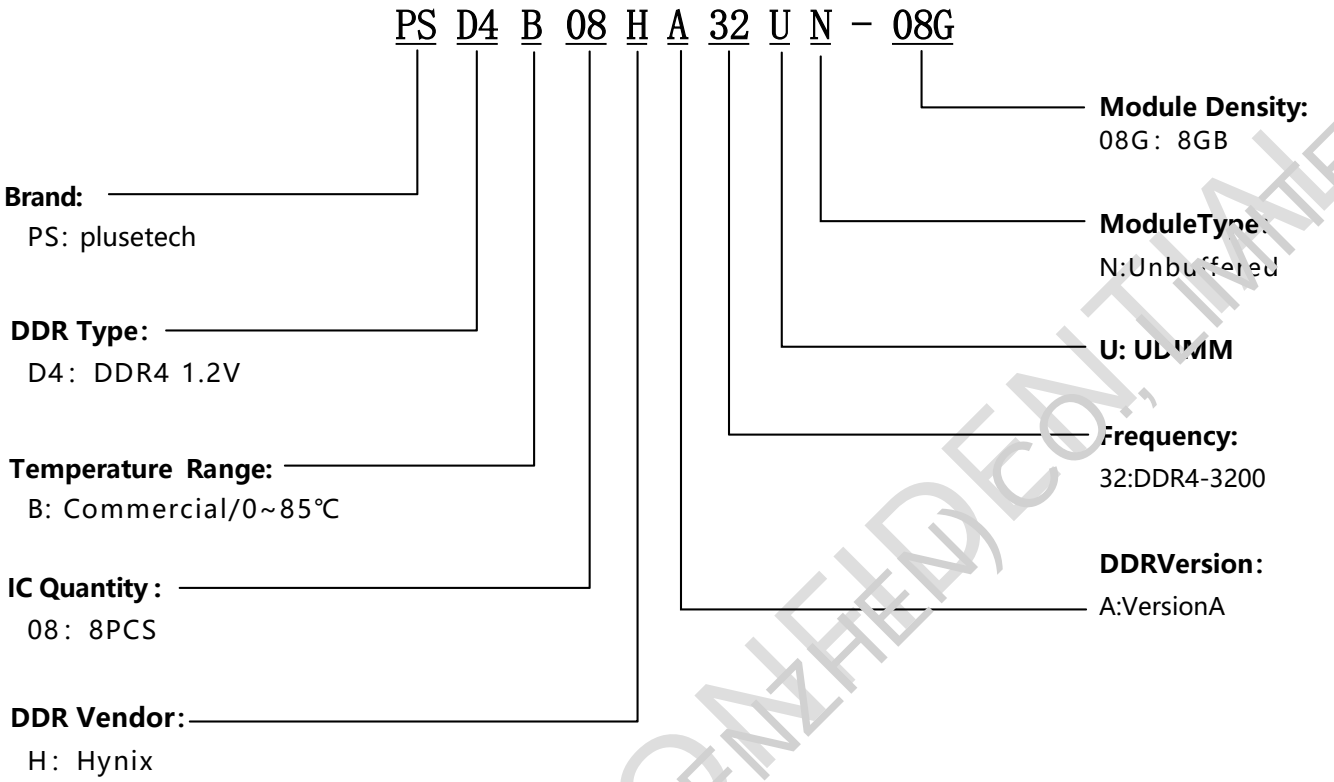


Notes:

1. All dimensions are in millimeters (mm), MAX/MIN or typical(TYP) where noted.
2. All dimensions diagrams is for reference only.

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Part Number Decode



Revision History

Rev.A0 – 12/22

- Initial release.

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