# Plusetech DDR5 16GB 5600 UDIMM Datasheet

# PSD5B08MA56UN-16G

| | |
|---|---|
| **Module Part Number** | PSD5B08MA56UN-16G |
| **Memory Type** | DDR5 |
| **Module Type** | Unbuffered DIMM |
| **Module Density** | 16GB |
| **Data Width** | x64 |
| **Data Rate** | 5600 MT/s |
| **$V_{DD}$ Voltage** | 1.1V |
| **Interface** | 288-pin |
| **Number of Ranks** | 1 |
| **SDRAM Device Width** | x8 |
| **CAS Latency** | CL46 |
| **Operation Temperature** | 0°C ~ +85°C |
| **RoHS** | Yes |
| **Standard** | JEDEC |

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# Features

- JEDEC Standard
- 288-pin, sunbuffered dual in-line memory module(UDIMM)
- Fast data transfer rates: PC5-5600, backward compatible PC4-4800.
- 16GB (2G x 8 x 8PCS)
- $V_{DD}/V_{DDQ}$ = 1.1V (-33mV / +66mV)
- $V_{pp}$ = 2.5V(-125mV / +250mV)
- 8 BG(Bank Group) for x4/x8/x16 configurations
- Single-rank
- 32 bank with x4/x8
- 16 bank with x16
- BL16, BC8 OTF, BL32, BL32 OTF supported
- Same Bank Refresh
- VrefDQ / VrefCA / VrefCS Training
- Per Pin VREFDQ Training
- Read / CA / CS Training Mode
- Hard/Soft Post Package Repair
- Maximum Power Saving Mode (MPSM)
- Multi-Purpose Command (MPC)
- Per DRAM Addressability (PDA)
- Connectivity Test (CT)
- ZQ Calibration
- DFE (Decision Feedback Equalization) for DQ
- DQS Interval Oscillator
- 1N / 2N Mode support for Commands
- Package Output Driver Test Mode
- On-Die ECC
- ECC Transparency and Error Scrub
- CRC (Cyclic Redundancy Check)
- JEDEC standard
  82ball FBGA(x8)
  106ball FBGA(x16)
- Gold edge contacts
- This product in compliance with the RoHS directive

**Options**

- Operation temperature
  - Commercial 0°C ~ +85°C
- Package
  - 288-pin DIMM
- Frequency/CAS latency
  - 0.357ns @ CL = 46(DDR5-5600BN)

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## Table 1: Ordering Information

| Part Number | Density | Rank | Voltage | Date rate | Component Composition | Clock cycles (CL-tRCD-tRP) |
|---|---|---|---|---|---|---|
| PSD5B08MA56UN-16G | 16GB | 1 | 1.1V | 5600 MT/s | 2Gx8*8 | 46-46-46 |

## Table 2: Addressing

| Parameter | 16GB |
|---|---|
| **Device Configuration** | 2Gb x 8bit * 8 pcs |
| **ROW address** | 128K (R[16:0]) |
| **Column address** | 1K (C[9:0]) |
| **Device bank group address** | 4 (BG[1:0]) |
| **Device bank address per group** | 4 (BA[1:0]) |
| **Page size** | 2KB |

## Table 3: DDR5-5600 Speed Bins

| Speed Bin | | DDR5-5600BN | | Unit | Note |
|---|---|---|---|---|---|
| CL - nRCD - nRP | | 46-46-46 | | | |
| Parameter | Symbol | min | max | | |
| Internal read command to first data | $t_{AA}$ | 16.00 | | ns | |
| ACT to internal read or write delay time | $t_{RCD}$ | 16.00 | - | ns | |
| PRE command period | $t_{RP}$ | 16.00 | - | ns | |
| ACT to ACT or REF command period | $t_{RC}$ | 48.00 | - | ns | |
| ACT to PRE command period | $t_{RAS}$ | 32.00 | 5 * $t_{REFI}$ | ns | |

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## Table4: Operating Conditions

### Recommended DC Operating Conditions — DDR5 (1.1V) operation

| Symbol | Parameter | Rating | | | Units | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{DD}$ | Device Supply Voltage | 1.067 | 1.1 | 1.166 | V | 1,2 |
| $V_{DD}Q$ | Supply Voltage for I/O | 1.067 | 1.1 | 1.166 | V | 1,2 |
| VPP | Core Power Voltage | 1.746 | 1.8 | 1.908 | V | 1,2 |

**Notes:**

1. VDD must be within 66mv of VDDQ.
2. AC parameters are measured with VDD and VDDQ tied together.

## Table 5: DRAM Component Operating Temperature Range

| Symbol | Parameter | Rating | Units | Notes |
|---|---|---|---|---|
| $T_{OPER}$ | Normal Operating Temperature Range | 0 to 85 | ℃ | 1,2 |

## Table 6: Absolute Maximum DC Ratings

| Symbol | Parameter | Rating | Units | Notes |
|---|---|---|---|---|
| $V_{DD}$ | Voltage on $V_{DD}$ pin relative to $V_{SS}$ | -0.3V~1.5V | V | 1,3 |
| $V_{DD}Q$ | Voltage on $V_{DD}Q$ pin relative to $V_{SS}$ | -0.3V~1.5V | V | 1,3 |
| $V_{pp}$ | Voltage on $V_{PP}$ pin relative to Vss | -0.3V~1.5V | V | 4 |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to $V_{SS}$ | -0.3V~1.5V | V | 1,3 |
| $T_{STG}$ | Storage Temperature | -55 to +100 | ℃ | 1,2 |

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# PCB Feature overview

- **General**

  * Board size: 133.35 x 31.25 mm ±0.15 mm

  * Finished Board Thickness: 1.27 ±0.1 mm

* Panel: 5 pieces PCB per panel

* **8-layer board**

  * Impedance: 30/40/55 Ohm ±10% (Single-ended)

    40/55 Ohm ±10% (Differential)

* **Pin count:** 288**PIN**

- **PCB Material**

* Glass Epoxy FR4, .UL 94V-0, BP ML

- **Plating**

* Edge Connector Plating: Nickel Followed by gold

- Nickel Plating Thickness: 100 u" min.
- Surface treatment:

  Gold Plating: 3u" min.

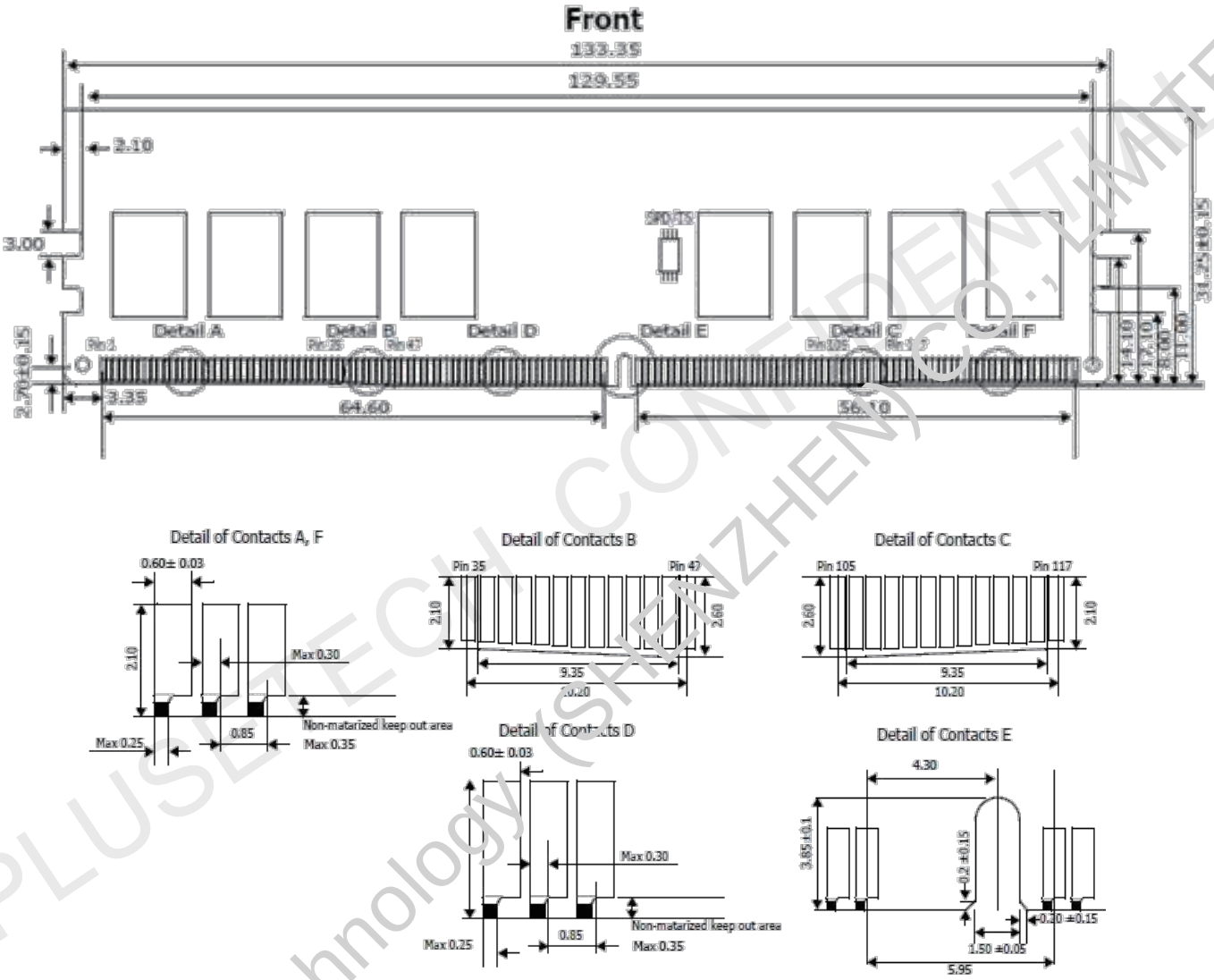
  SMT PAD: average 2~3u"

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# Module Dimensions

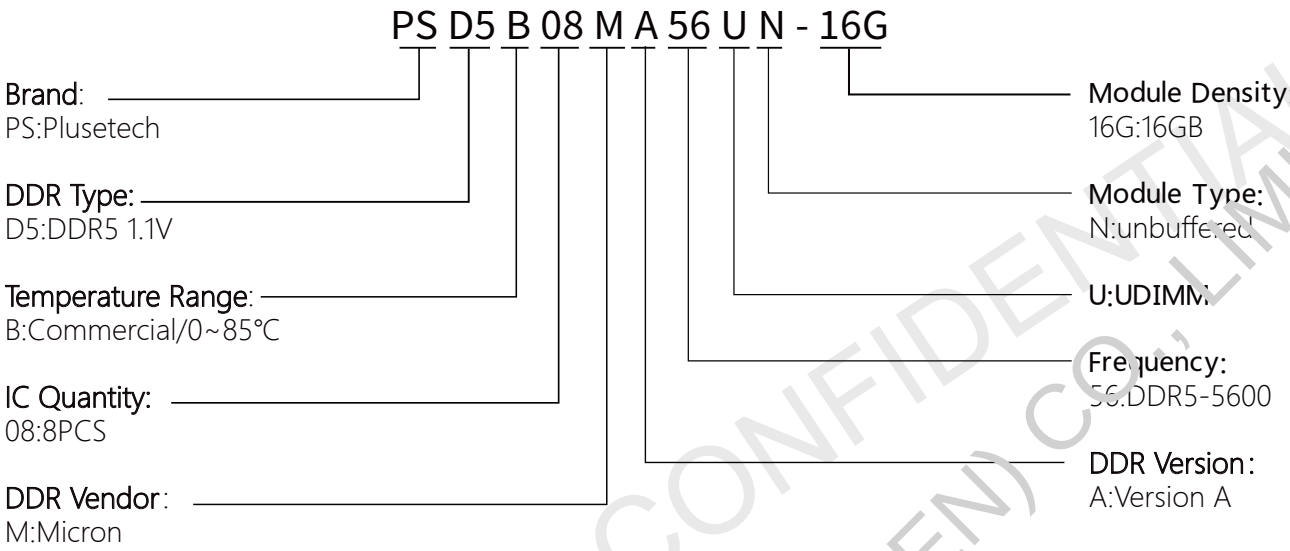
## Figure 1: 288-pin DDR5 UDIMM




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## Part Number Decode




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## Revision History

**Rev.A0 — 12/22**

- Initial release.

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