315ball FBGA Specification

32Gb LPDDR5 (x32)

PSL5M0D7S-032G

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Revision History

Version	Date	Description
1.0	2026/01	First Release

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1. INTRODUCTION

1.1 Product Information

Part ID	Capacity	Size	Package
PSL5M0D7S-032G	32Gb	12.4*15mm	FBGA315

Table 1 Product Information

1.2 Part Number Chart

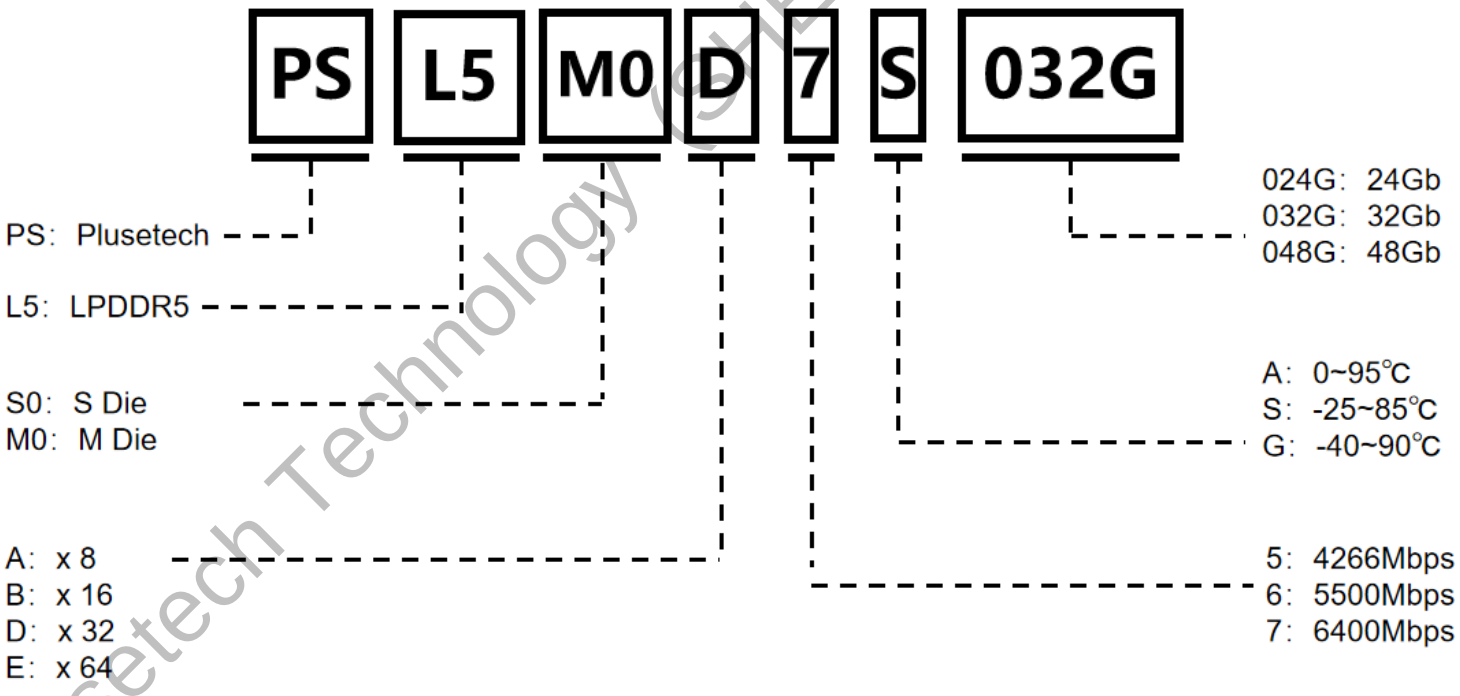


Figure 1 Part Number Chart

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1.3 Features

- **Architecture**
- 12.8GB/s maximum bandwidth per channel
- Frequency range: 800–5 MHz (data rate range per pin: 6400–40 Mb/s with WCK:CK = 4:1)
- Selectable CKR (WCK:CK = 2:1 or 4:1)
- **LPDDR5/5X data interface**
- Single x16 channel/die
- Double-data-rate command/address entry
- Differential command clocks (CK_t/ CK_c) for high-speed operation
- Differential data clocks (WCK_t/WCK_c)
- Optional differential read strobe (RDQS_t/RDQS_c)
- 16*n*-bit or 32*n*-bit prefetch architecture
- 4KB page size with 8-bank (8B mode), 2KB page size with bank group (BG mode), or 16-bank (16B mode) operation
- Command-selectable burst lengths (BL= 16 or 32) in bank group or 16-bank modes
- Background ZQ calibration/command-based ZQ calibration
- Optional link protection (link ECC)
- Partial-array self refresh (PASR) and partial- array auto refresh (PAAR) with segment mask
- **Ultra-low-voltage core and I/O power supplies**
- V_{DD1} = 1.70–1.95V; 1.8V NOM
- V_{DD2H} = 1.01–1.12V; 1.05V NOM
- V_{DD2L} = V_{DD2H} or 0.87–0.97V; 0.9V NOM
- V_{DDQ} = 0.5V NOM or 0.3V NOM (ODT off)
- Interface-LVSTL 0.5/0.3
- I/O type: Low-swing single-ended, VSS terminated
- VOH-compensated output drive
- Programmable VSS on-die termination (ODT)
- Non target ODT support
- DVFSQ support
- Per byte and per pin DFE support
- **Low power features**
- DVFSC: Dynamic voltage frequency scaling core
- Single-ended CK, single-ended WCK and single-ended RDQS
- Data copy
- Write X
- **V_{DD1}/V_{DD2H}/V_{DD2L}/V_{DDQ} (ODT on)/ (ODT off):**

  1.8V/1.05V/0.9V/0.5V/0.3V
- **Array configuration**
- 1Gig x 32 (1G x 16 x 2Ch) 1G32
- **Device configuration**
- 2 die in package (1G16 x 2 die) D2
- **FBGA RoHS-compliant "green" package**
- 315-ball FBGA (12.4mm × 15mm), seated height 1.0mm (MAX)
- **Speed grade, cycle time (tWCK)**
- 6400 Mb/s
- **Operating temperature**
- –25°C to +85°C

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1.4 Device Configuration

Item	Description	1G32 (32Gb/package)		
Die Organization	Channel A, rank 0	x16 mode × 1 die		
	Channel B, rank 0	x16 mode × 1 die		
	Channel A, rank 1	-		
	Channel B, rank 1	-		
Die Addressing	Density per die	16Gb		
	Bits	17,179,869,184		
	Bank mode	BG mode	16B mode	8B mode
	Configuration	64Mb × 16 DQ × 4 Banks × 4BG	64Mb × 16 DQ × 16 Banks	128Mb × 16 DQ × 8 Banks
	Number of banks	4	16	8
	Number of bank groups	4	1	1
	Array prefetch bits	256	256	512
	Rows per bank	65,536		
	Columns	64		
	Page size (bytes)	2048	2048	4096
	Native burst length	16	16	32
	Number of I/Os	16		
	Bank address	BA[1:0]	BA[3:0]	BA[2:0]
	Bank group address	BG[1:0]	–	–
	Row address	R[15:0]		
	Column address	C[5:0]		
	Burst address	B[3:0]	B[3:0]	B[4:0]
	Burst starting address boundary	128-bit		

Table 2 Die Organization and Addressing in the Package

Notes:
1. Refer to the SDRAM Addressing section in General LPDDR5/5X Specification 3.
2. Refer to the Speed Grades and Effective Burst Length in General LPDDR5/5X Specifications.

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1.5 Refresh Requirement Parameters

Parameter	Symbol	16Gb Die		Unit
		BG and 16B Mode	8B Mode	
REFRESH cycle time (all banks)	^{t}RFCab	280	280	ns
REFRESH cycle time (per bank)	^{t}RFCpb	140	140	ns
Per bank refresh to per bank refresh time (different bank)	^{t}PBR2PBR	90	90	ns
Per bank refresh to ACTIVATE command time (different bank)	^{t}PBR2ACT	7.5	10	ns

Table 3 Refresh Requirement Parameters

Note:

This table only describes refresh parameters that are density dependent. Refer to Refresh Requirement section in General LPDDR5/LPDDR5X Specifications 3 for all refresh parameters.

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1.6 Package Block Diagrams

Dual Die, Dual Channel, Dual-Rank

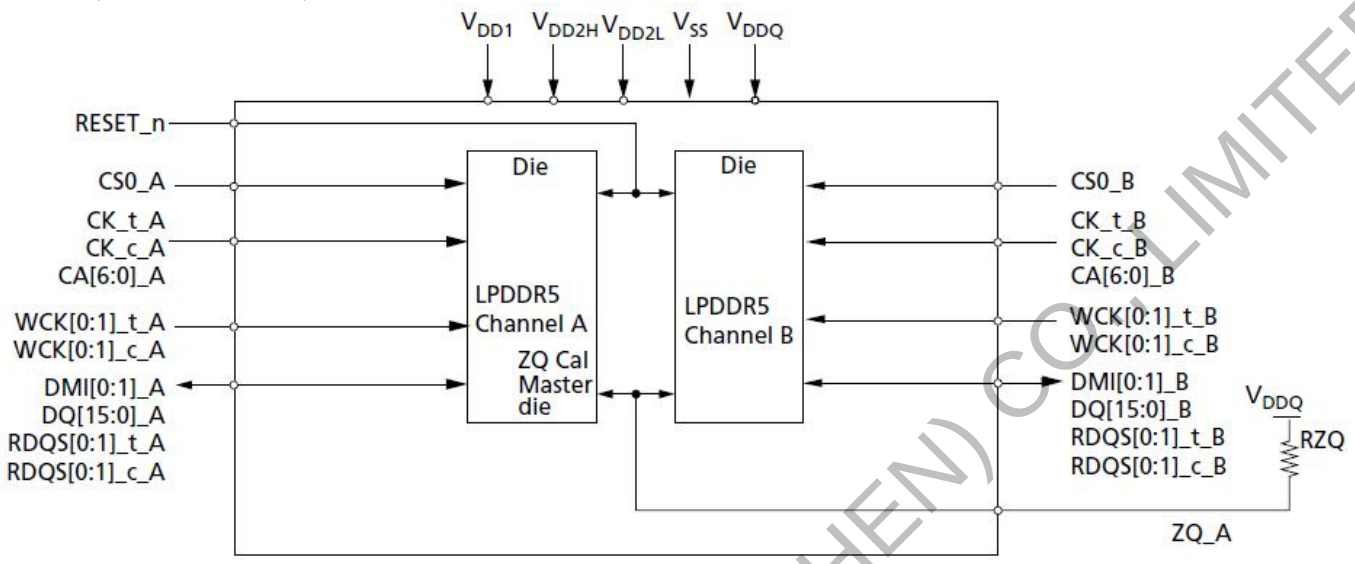
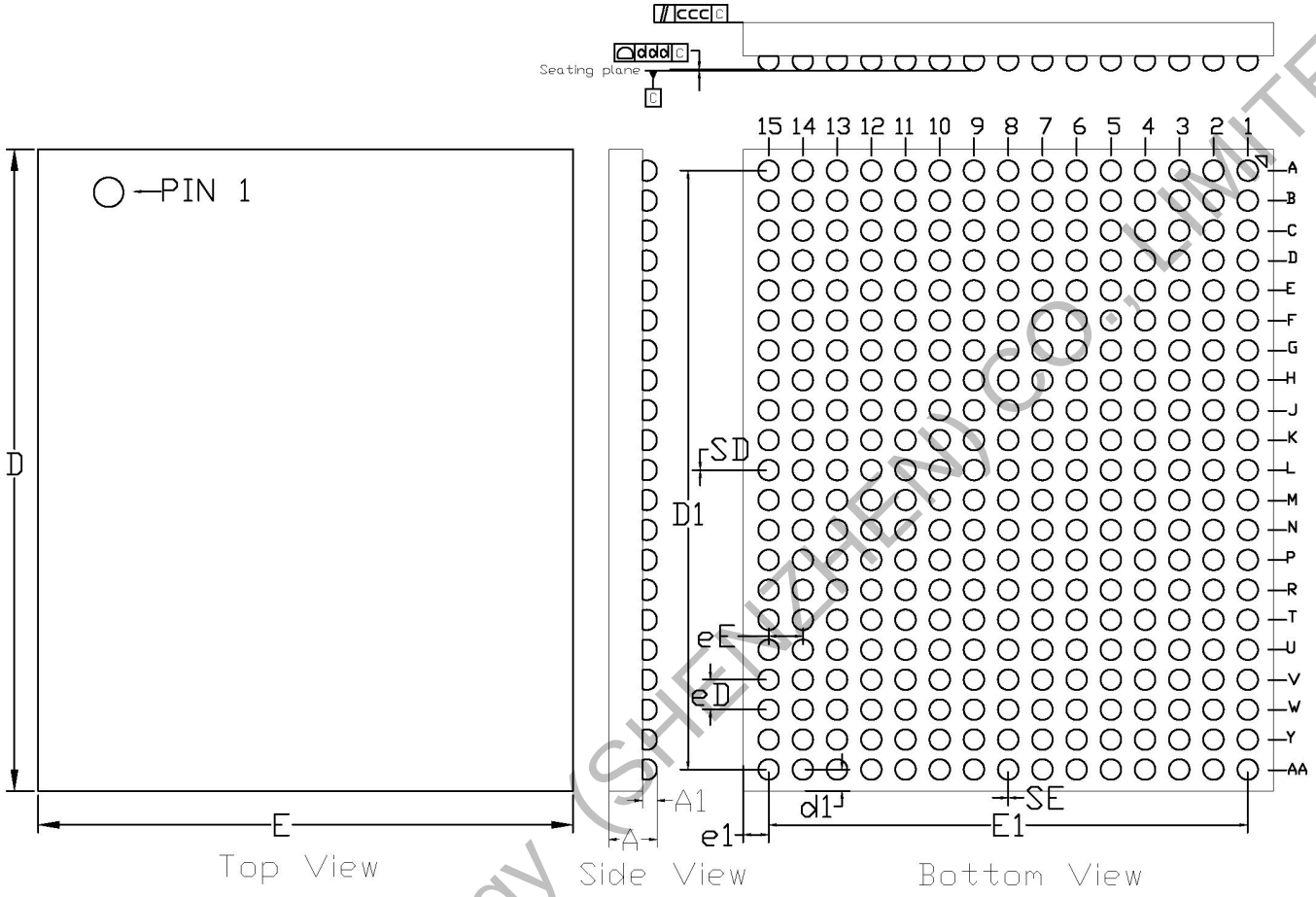


Figure 2 Dual-Die, Dual-Channel, Dual-Rank Package Block Diagram

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1.7 Package Dimension



ITEM	Symble	Unit: mm MIN	NORM	MAX
BODY SIZE	D	14.90	15.00	15.10
	E	12.30	12.40	12.50
TOTAL THICNESS	A	0.80	0.90	1.00
STAND OFF	A1	0.27	0.30	0.33
EDGE BALL (CENTER TO CENTER)	D1		14.00	
	E1		11.20	
BALL PITCH	eD		0.70	
	eE		0.80	
even number of balls (eE/2,eD/2) odd number of balls (0)	SE		0	
	SD		0	
BALL COUNT	n		315	
BALL WIDTH(after reflow)	ΦA	0.47	0.50	0.53
BALL TO OUTLINE	d1	0.40	0.50	0.60
	e1	0.50	0.60	0.70
Mold package warpage	ccc			0.10
COPLANARITY	ddd			0.08
JEDEC	MO-338A			

Notice: 1.Ball diameter: 0.45mm (Before Reflow)
2."●"---bumping ball location
3.In the diagram,there are 315 ball locations in all.

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Figure 3 Package Dimension (12.4mm*15mm*1.0mm max)

1.8 Ball Assignment

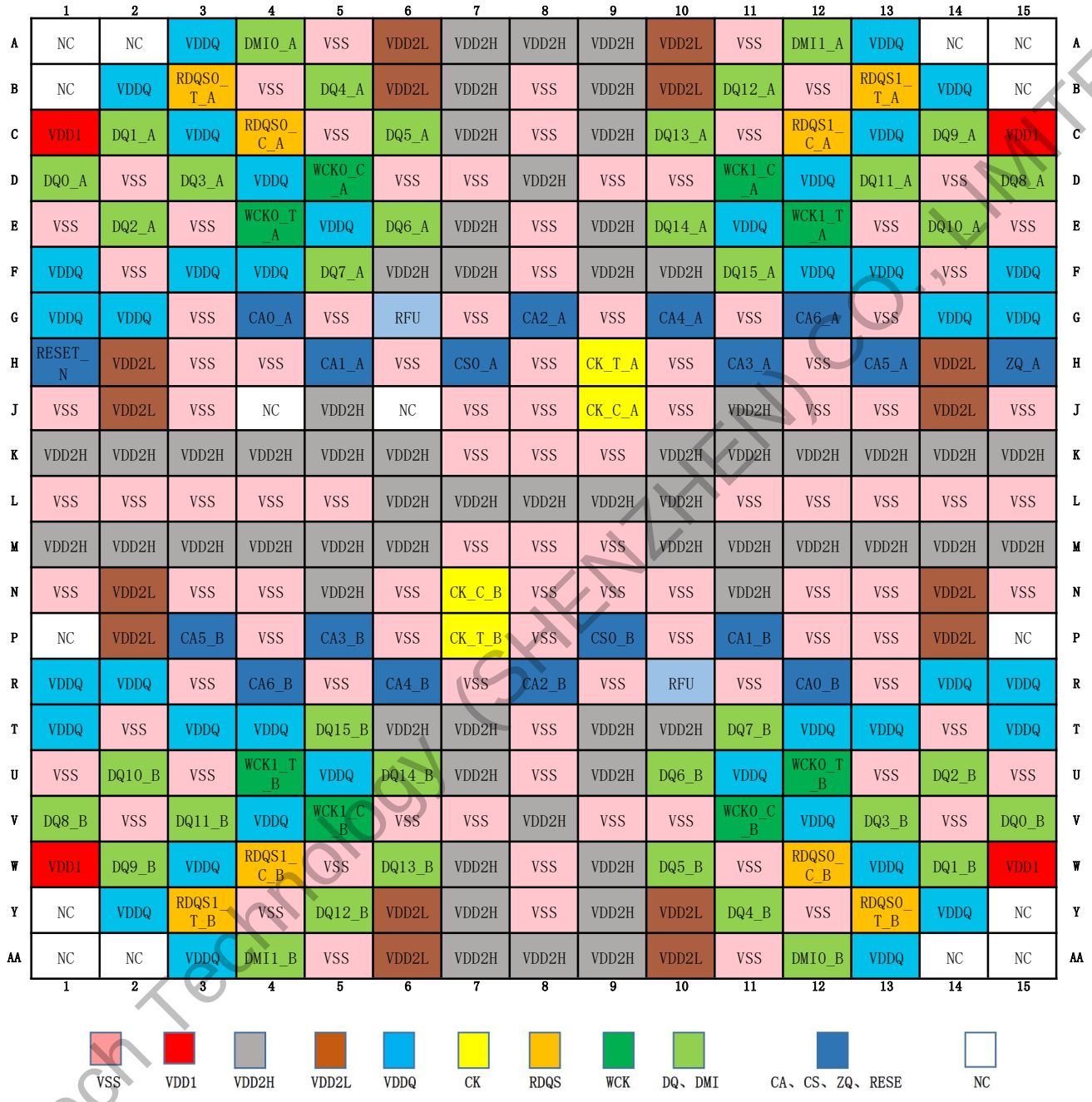


Figure 4 315-Ball Dual-Channel Discrete BGA

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1.9 PIN Description

Symbol	Type	Description
CK_t_[A:B] CK_c_[A:B]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:B], CS1_[A:B]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] become NC pins in a single-rank package.
CA[6:0]_[A:B]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:B] WCK[1:0]_c_[A:B]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_[A:B]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A:B] RDQS[1:0]_c_[A:B]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:B]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240Ω ±1% resistor.
VDDQ, VDD1 , VDD2H , VDD2L	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
VSS	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.
RFU	-	**RFU:** Reserved for future use on larger capacity configurations.

Table 4 Ball/Pad Description

Note:
CS1_A, and CS1_B balls are reserved for 2-rank package. For 1-rank package those balls are RFU.

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1.10 Mode Register Definition

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0	**Per-pin DFE**	**Pre Emphasis**	**Unified NT ODT behavior mode**	**DMI output behavior mode**	**Optimized refresh mode**	**Enhanced WCK always-on mode**	**Latency mode**	**NT ODT timing mode**
	OP[0] = 1b: Device supports different NT ODT latency for DQ and RDQS							
	OP[1] = 0b: Device supports x16 mode latency							
	OP[2] = 1b: Device supports enhanced WCK always-on mode							
	OP[3] = 1b: Device supports optimized refresh mode							
	OP[4] = 1b: Device supports both DMI behavior mode 1 and 2 and mode selection							
	OP[5] = 1b: The NT ODT behavior follows the unified NT ODT behavior							
	OP[6] = 1b: Device supports Pre Emphasis mode							
	OP[7] = 0b: Device does not support Per Pin DFE							
MR1							**ARFM support[3]**	**CS ODT OP support**
	OP[0] = 0b: Device supports CS ODT behavior OP							
	OP[1] = 1b: Device supports ARFM							
MR3				**BK/BG Org**				
	OP[4:3] = 00b: BG, 01b: 8B, 10b: 16B Mode Supported							
MR5	**Manufacturer ID**							
	1111 1111b							
MR6	**Revision ID1**							
	0000 0111b							
MR8	**I/O width**			**Density**				**Type**
	OP[7:6] = 00b: x16			OP[5:2] = 0110b: 16Gb				OP[1:0] = 01b: LPDDR5X SDRAM
MR13						**VRO**		
	OP[2] = 0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6							
MR19			**WCK2DQ OSC FM**					
	OP[5] = 1b: WCK2DQ OSC FM supported							

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Mode Register Definition (Continued)

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR21	**WXS**				**ODTD-CSFS**	**WXFS**	**RDCFS**	**WDCFS**
	OP[0] = 1b: WRITE DATA COPY function supported							
	OP[1] = 1b: READ DATA COPY function supported							
	OP[2] = 1b: WRITE X function supported							
	OP[3] = 1b: Device ODTD-CS is supported							
	OP[7] = 1b: Data to be written can be selected with 0 and 1							
MR22	**RECC**			**WECC**				
	OP[5:4] = 00b: Write link ECC disabled (default) 01b: Write link ECC enabled (See Note 4)							
	OP[7:6] = 00b: Read link ECC disabled (default) 01b: Read link ECC enabled (See Note 4)							
MR24	**DFES**				**Read DCA**			
	Op[3] = 1b: Device supports Read DCA							
	Op[7] = 1b: Device supports DFE (see Note 5)							
MR26		**RDQSTFS**						
	OP[6] = 1b: Read/write-based RDQS_t TRAINING function supported							
MR27	**RAAMULT**			**RAAIMT**				**RFM**
	OP[0] = 1b: RFM is required							
	OP[5:1] = 01110b: 112							
	OP[7:6] = 01b: 4X							
MR43		**SBEC rule**						
	OP[6] = 1b: Simultaneous SBE on each DQ byte and DMI are independently counted							
MR57	**ARFM**[3]				**RFMSB**		**RAADEC**	
	OP[1:0] = 10b: 2 × RAAIMT							
	OP[3:2] = 00b: Single Bank Mode not supported							
	OP[7:6] = 00b: default (01110b: 112), 01b: Level A = 01101b: 104, Level B = 01100b: 96, Level C = 01011: 88							

Table 5 Mode Register Contents

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Notes:

1. The contents of mode registers described here reflect information specific to each die in these packages.
2. Refer to General LPDDR5/LPDDR5X Specification 1 for mode registers not described here.
3. Refer to General LPDDR5/LPDDR5X Specification 3 for feature description not described here.
4. Write link ECC and read link ECC are supported.
5. Device supports 3-step DFE.

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2. I_{DD} Parameters

2.1 I_{DD} Specification

Parameter/Condition	Symbol	Power Supply	Note
Operating one bank active-precharge current: tCK = tCK, min; tRC = tRC, min; CS is LOW between valid commands; CA bus inputs are switching: Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled) ODT disabled; WCK inputs are stable.	I_{DD01}	V_{DD1}	-
	I_{DD02H}	V_{DD2H}	9
	I_{DD02L}	V_{DD2L}	-
	I_{DD0Q}	V_{DDQ}	3
Idle power-down standby current: tCK = tCK, min; POWER-DOWN command is issued; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled) ODT is disabled WCK in-puts are stable.	I_{DD2P1}	V_{DD1}	-
	I_{DD2P2H}	V_{DD2H}	
	I_{DD2P2L}	V_{DD2L}	
	I_{DD2PQ}	V_{DDQ}	3
Idle power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CS is LOW; All banks are idle; CA bus in-puts are stable; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable.	I_{DD2PS1}	V_{DD1}	-
	$I_{DD2PS2H}$	V_{DD2H}	
	$I_{DD2PS2L}$	V_{DD2L}	
	I_{DD2PSQ}	V_{DDQ}	3
Idle non power-down standby current: tCK = tCK, min; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable.	I_{DD2N1}	V_{DD1}	-
	I_{DD2N2H}	V_{DD2H}	
	I_{DD2N2L}	V_{DD2L}	
	I_{DD2NQ}	V_{DDQ}	3
Idle non power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CS is LOW; All banks are idle; CA bus in-puts are stable; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable.	I_{DD2NS1}	V_{DD1}	-
	$I_{DD2NS2H}$	V_{DD2H}	
	$I_{DD2NS2L}$	V_{DD2L}	
	I_{DD2NSQ}	V_{DDQ}	3
Active power-down standby current: tCK = tCK, min; CS is LOW; One bank is active; POWERDOWN ENTRY command is issued; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable.	I_{DD3P1}	V_{DD1}	9
	I_{DD3P2H}	V_{DD2H}	
	I_{DD3P2L}	V_{DD2L}	
	I_{DD3PQ}	V_{DDQ}	3
Active power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CS is LOW; One bank is active; CA bus in-puts are stable; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable and static.	I_{DD3PS1}	V_{DD1}	9
	$I_{DD3PS2H}$	V_{DD2H}	
	$I_{DD3PS2L}$	V_{DD2L}	8, 9
	I_{DD3PSQ}	V_{DDQ}	4

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Parameter/Condition	Symbol	Power Supply	Note
Active non power-down standby current: tCK = tCK, min; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable and static.	I_{DD3N1}	V_{DD1}	9
	I_{DD3N2H}	V_{DD2H}	
	I_{DD3N2L}	V_{DD2L}	8, 9
	I_{DD3NQ}	V_{DDQ}	4
Active non power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CS is LOW; One bank is active; CA bus in-puts are stable; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable and static.	I_{DD3NS1}	V_{DD1}	9
	$I_{DD3NS2H}$	V_{DD2H}	
	$I_{DD3NS2L}$	V_{DD2L}	8, 9
	I_{DD3NSQ}	V_{DDQ}	4
Operating burst READ current BG mode: tCK = tCK,min; tWCK = tWCK, min; CS is LOW between valid commands.**One bank in each bank group 1 and 2 is active;** BL = 16 or 32; RL = RL,min; CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled.	I_{DD4R1}	V_{DD1}	-
	I_{DD4R2H}	V_{DD2H}	
	I_{DD4R2L}	V_{DD2L}	8
	I_{DD4RQ}	V_{DDQ}	5
Operating burst READ current 8B/16B mode: tCH = tCK, min; tWCK = tWCK, min; CS is LOW between valid commands. **One banks is active;** BL = 16 or 32 for 16B, BL32 for 8B; RL = RL, min; CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled.	I_{DD4R1}	V_{DD1}	-
	I_{DD4R2H}	V_{DD2H}	
	I_{DD4R2L}	V_{DD2L}	8
	I_{DD4RQ}	V_{DDQ}	5
Operating burst WRITE current BG mode: tCK = tCK, min; tWCK = tWCK, min; CS is LOW between valid commands. **One bank in each bank group 1 and 2 is active**; BL = 16 or 32; W L= WL,min; CA bus inputs are switching; 50% data change each burst transfer; RDQS_t is stable (if Link ECC is enabled); ODT is disabled.	I_{DD4W1}	V_{DD1}	-
	I_{DD4W2H}	V_{DD2H}	
	I_{DD4W2L}	V_{DD2L}	8
	I_{DD4WQ}	V_{DDQ}	4
Operating burst WRITE current 8B/16B mode: tCH = tCK, min; tWCK = tWCK, min; CS is LOW between valid commands.**One banks is active;** BL = 16 or 32 for 16B, BL32 for 8B; WL = WL,min; CA bus inputs are switching; 50% data change each burst transfer; RDQS_t is stable (if Link ECC is enabled); ODT is disabled.	I_{DD4W1}	V_{DD1}	-
	I_{DD4W2H}	V_{DD2H}	
	I_{DD4W2L}	V_{DD2L}	8
	I_{DD4WQ}	V_{DDQ}	4
All-bank REFRESH burst current: tCH = tCK, min; CS is LOW between valid commands; tRC = tRFCab, min; Burst refresh; CA bus inputs are switching; Data bus in-puts are stable; ODT is disabled; WCK inputs are stable and static.	I_{DD51}	V_{DD1}	-
	I_{DD52H}	V_{DD2H}	
	I_{DD52L}	V_{DD2L}	8
	I_{DD5Q}	V_{DDQ}	4
All-bank REFRESH average current: tCH = tCK, min; CS is LOW between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable and static.	I_{DD5AB1}	V_{DD1}	-
	$I_{DD5AB2H}$	V_{DD2H}	
	$I_{DD5AB2L}$	V_{DD2L}	8
	I_{DD5ABQ}	V_{DDQ}	4

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Parameter/Condition	Symbol	Power Supply	Note
Per-bank REFRESH average current: tCH = tCK, min; CS is LOW between valid commands; tRC = tREFI/8; CA bus inputs areswitching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable and static.	I_{DD5PB1}	V_{DD1}	-
	$I_{DD5PB2H}$	V_{DD2H}	
	$I_{DD5PB2L}$	V_{DD2L}	8
	I_{DD5PBQ}	V_{DDQ}	4
Power-down self refresh current: CK_t = LOW, CK_c = HIGH; CS is LOW; CA bus inputs are stable; Data bus inputs are stable; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable and static.	I_{DD61}	V_{DD1}	6, 7
	I_{DD62H}	V_{DD2H}	
	I_{DD62L}	V_{DD2L}	
	I_{DD6Q}	V_{DDQ}	4, 6, 7
Deep-sleep mode current: CK_t = LOW, CK_c = HIGH; CS is LOW; CA bus inputs are stable; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled); ODT is disabled; WCK inputs are stable and static.	I_{DD6DS1}	V_{DD1}	6, 7
	$I_{DD6DS2H}$	V_{DD2H}	
	$I_{DD6DS2L}$	V_{DD2L}	
	I_{DD6DSQ}	V_{DDQ}	4, 6, 7

Table 6 IDD Specification

Note:

1. Published IDD values are the maximum IDD values considering the worst case conditions of process, temperature, and voltage.
2. ODT disabled MR11 op[6:4] = 000b
3. IDD current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of V DDQ andVDD2H/V DD2L.
5. Guaranteed by design with an output load = 5pF and RON = 40 ohm.
6. The 1x self refresh rate is the rate that the LPDDR5 device is refreshed internally during self refresh before going into the elevated temperature range.
7. This is the general definition that applies to full-array self refresh.
8. When MR13 OP[7] is high, single V DD2 rail, V DD2L current shall be added to V DD2H cur-rent.
9. IDD values can be different according to the bank organization set by MR3 OP[4:3].
10. When DVFSC is enabled, the minimum tCK shall be set by following the DVFSC operating frequency.

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2.2 I_{DD} Parameters for Single Die

V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V;
T_C= –25°C to +85°C

Symbol	Supply	Speed Grade 6400Mb/s x16	Unit	Note
IDD01	VDD1	3.20	mA	2
IDD02H	VDD2H	29.00		
IDD02L	VDD2L	0.20		
IDD0Q	VDDQ	0.60		
IDD2P1	VDD1	1.50	mA	2
IDD2P2H	VDD2H	2.50		
IDD2P2L	VDD2L	0.20		
IDD2PQ	VDDQ	0.60		
IDD2PS1	VDD1	1.50	mA	2
IDD2PS2H	VDD2H	2.50		
IDD2PS2L	VDD2L	0.20		
IDD2PSQ	VDDQ	0.60		
IDD2N1	VDD1	1.50	mA	2
IDD2N2H	VDD2H	17.00		
IDD2N2L	VDD2L	0.20		
IDD2NQ	VDDQ	0.60		
IDD2NS1	VDD1	1.50	mA	2
IDD2NS2H	VDD2H	17.00		
IDD2NS2L	VDD2L	0.20		
IDD2NSQ	VDDQ	0.60		
IDD3P1	VDD1	1.50	mA	2
IDD3P2H	VDD2H	6.50		
IDD3P2L	VDD2L	0.20		
IDD3PQ	VDDQ	0.60		
IDD3PS1	VDD1	1.50	mA	2
IDD3PS2H	VDD2H	6.50		
IDD3PS2L	VDD2L	0.20		
IDD3PSQ	VDDQ	0.60		
IDD3N1	VDD1	1.80	mA	2
IDD3N2H	VDD2H	21.00		
IDD3N2L	VDD2L	0.20		
IDD3NQ	VDDQ	0.60		
IDD3NS1	VDD1	1.80	mA	2
IDD3NS2H	VDD2H	21.00		
IDD3NS2L	VDD2L	0.20		
IDD3NSQ	VDDQ	0.60		
IDD4R1	VDD1	11.00	mA	2, 3, 4
IDD4R2H	VDD2H	435.00		
IDD4R2L	VDD2L	0.20		
IDD4RQ	VDDQ	116.00		
IDD4W1	VDD1	10.00	mA	2, 3
IDD4W2H	VDD2H	305.00		
IDD4W2L	VDD2L	0.20		
IDD4WQ	VDDQ	0.60		

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Symbol	Supply	Speed Grade 6400Mb/s	Unit	Note
		x16		
IDD51	VDD1	23.00	mA	2
IDD52H	VDD2H	165.00		
IDD52L	VDD2L	0.20		
IDD5Q	VDDQ	0.60		
IDD5AB1	VDD1	3.20	mA	2
IDD5AB2H	VDD2H	27.00		
IDD5AB2L	VDD2L	0.20		
IDD5ABQ	VDDQ	0.60		
IDD5PB1	VDD1	3.20	mA	2
IDD5PB2H	VDD2H	27.00		
IDD5PB2L	VDD2L	0.20		
IDD5PBQ	VDDQ	0.60		

Table 7 IDD Parameters

Note:
1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode. DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF, RON = 40 ohm, TC = 25°C.

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2.3 Full-Array Power-Down Self Refresh Current for Single Die

V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V;
T_C = –25°C to +85°C

Temperature	Symbol	Supply	Value	Unit	Note
25°C	I_{DD61}	V_{DD1}	0.27	mA	-
	I_{DD62H}	V_{DD2H}	0.60		
	I_{DD62L}	V_{DD2L}	-	µA	3
	I_{DD6Q}	V_{DDQ}	-		
	I_{DD6DS1}	V_{DD1}	0.27	mA	-
	$I_{DD6DS2H}$	V_{DD2H}	0.60		
	$I_{DD6DS2L}$	V_{DD2L}	-	µA	3
	I_{DD6DSQ}	V_{DDQ}	-		
85°C	I_{DD61}	V_{DD1}	3.30	mA	-
	I_{DD62H}	V_{DD2H}	13.00		
	I_{DD62L}	V_{DD2L}	0.20		-
	I_{DD6Q}	V_{DDQ}	0.60		
	I_{DD6DS1}	V_{DD1}	3.30		-
	$I_{DD6DS2H}$	V_{DD2H}	13.00		
	$I_{DD6DS2L}$	V_{DD2L}	0.20		-
	I_{DD6DSQ}	V_{DDQ}	0.60		

Table 8 Full-Array Current for Singe Die

Note:
1. I_{DD6} 25°C is the typical value in the distribution with nominal V_{DD} and a reference only value. I_{DD6} 85°C is the maximum I_{DD} guaranteed value considering the worst case conditions of process, temperature, and voltage.
2. DVFSC and DVFSQ disabled.
3. VDD2L and VDDQ power rails are not used during power-down self refresh.

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