LGA-8 (6x8mm) Specification

SD NAND 1Gbit
128MB Serial NAND

PSSD01G-WJ

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1. Overview

1.1 Product Description

SD NAND are highly integrated flash memories with serial and random access capability. It can be used in devices that support the SD2.0 standard. It is accessible via a dedicated serial interface optimized for fast and reliable data transmission.

The purpose of product development is to make memory chips based on the SD interface more stable and applicable to more scenarios. SD NAND is compatible with more MCUs with stable quality and strong compatibility, and can perfectly replace previous storage products based on SDIO interface. Its low power consumption is suitable for handheld products, and the rigorous production process makes it adaptable to diverse application scenarios.

1.2 Features Summary

-Capacity: 1Gbit (128MB)
- Complies with SD Specification 2.0
-Supports SD and SPI Mode
-Voltage range for communication: 2.7～3.6V
-Variable clock rate 0-25 MHz (standard), 0-50 MHz (high performance)
-Up to 18 MB/sec sequential read data transfer rate (using four parallel data lines)
-Password protection (CMD42-LOCK_UNLOCK)
-Sophisticated error recovery system with powerful ECC engine
-Global Wear Leveling
-Bad block management;
-Program/Erase:100,000 cycles typical (SLC NAND Flash)
-Power management for low power operation

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2. Pin Assignment

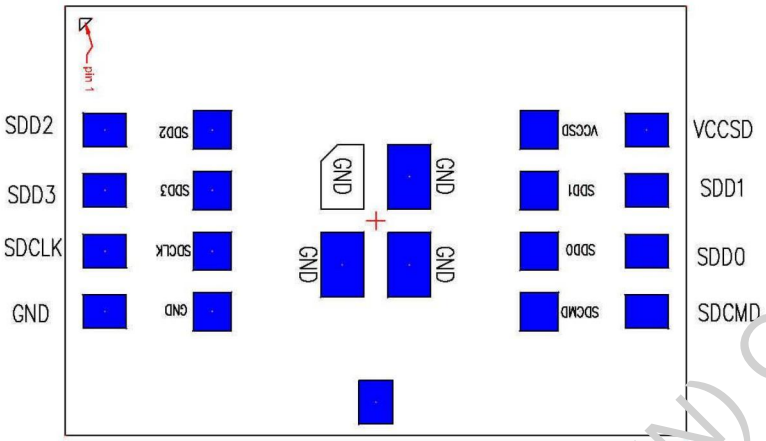


Figure 1:Top View

	SD Mode		SPI Mode	
Name	Type	Description	**Type**	**Description**
DAT2	I/O/PP	Data Line [Bit2]	RSV	Reserved
DAT3	I/O/PP	Data Line [Bit3]	I	Chip select(active low)
CLK	I	Clock	I	Clock
GND	S	Supply voltage ground	S	Supply voltage ground
VDD	S	Supply voltage	S	Supply voltage
DAT1	I/O/PP	Data Line [Bit1]	RSV	Reserved
DAT0	I/O/PP	Data Line [Bit0]	OPP	Data Out
CMD	PP	Command/Response	I	Data In

Table 1: Pin Assignment

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3. Product List

Product model	Capacity	Actual Size	Sequential R/W	Package
PSSD01G-WJ	128MB (1Gbit)	120MB	18/5 MB/S	6*8 (mm)

Table 2: Product List

4. Current Consumption

Standby current: 1.0mA(Maximum value)

Standby current: 0.8mA(average value)

Operating current: 30mA (maximum value)

Operating current: 25mA(average value)

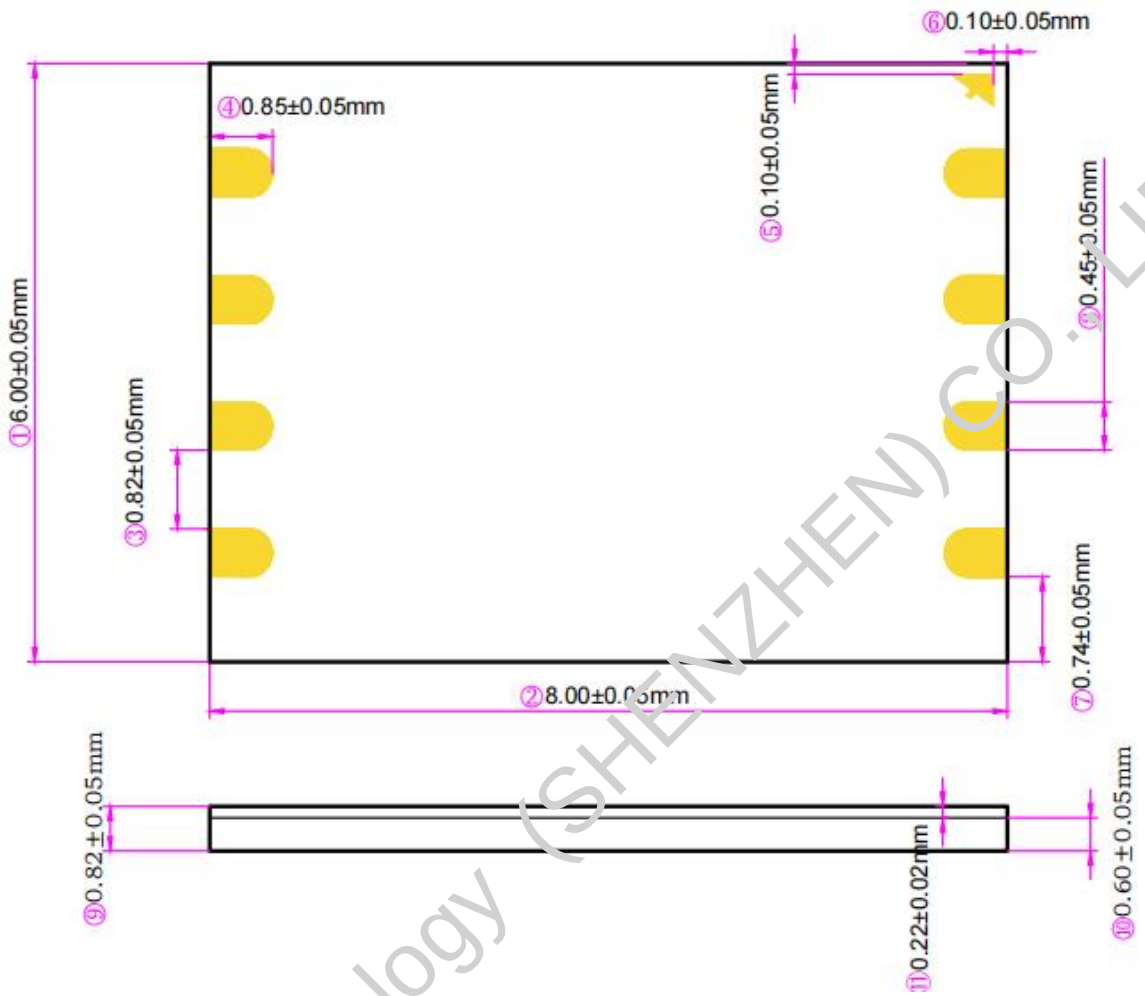
5. Operational Environment

Parameter	Range	
Temperature	Operating	0℃~70℃
	Non-Operating	-20℃~80℃
Humidity	Operating	25% to 85%, non-condensing
	Non-Operating	25% to 85%, non-condensing
Electrostatic Discharge (ESD)	IEC 61000-4-2 contact discharge: +/- 2[kV] and +/- 4[kV] 150[pF],330[Ohm] air discharge: up to +/- 15[kV] 150[pF], 330[Ohm]	

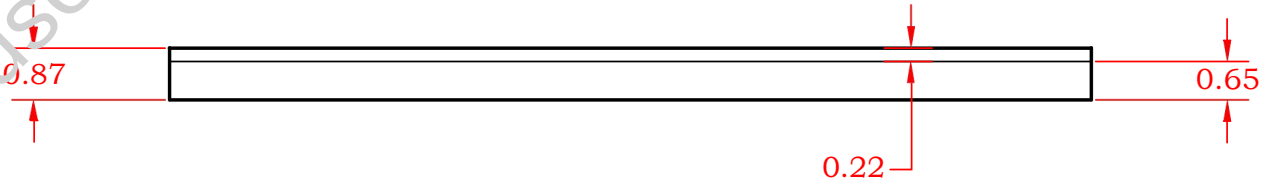
Table 3: Operational Environment

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6. Physical Dimension



Top View



Side view

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Top View
- Package length: 8.00 mm
- Package width: 6.00 mm
- Pin pitch: 1.27 mm
- Pin 1 marker: top-left corner
- Total 8 contacts, LGA package

Side View
- Typical package thickness: 0.75 mm
- Maximum package thickness: 0.80 mm

Pin layout corresponds to the pin definition defined in Chapter 2, conforming to the standard LGA-8 6×8mm SD NAND package specification.

Item	Dimension Description	Nominal Value	Tolerance	Note
①	Total Package Width	6.00	±0.05 mm	Package body width
②	Total Package Length	8.00	±0.05 mm	Package body length
③	Pad Pitch	0.82	±0.05 mm	Center-to-center spacing of adjacent pads
④	Pad Length	0.85	±0.05 mm	Gold finger pad length
⑤	Pin1 Marker Y-Offset	0.10	±0.05 mm	Distance from Pin1 marker to top edge
⑥	Pin1 Marker X-Offset	0.10	±0.05 mm	Distance from Pin1 marker to right edge
⑦	Bottom Pad Edge Clearance	0.74	±0.05 mm	Distance from bottom pad to package bottom edge
⑧	Pad Width	0.45	±0.05 mm	Gold finger pad width
⑨	Total Package Thickness	0.82	±0.05 mm	Overall package thickness
⑩	Molding Compound Thickness	0.60	±0.05 mm	Epoxy molding layer thickness
⑪	Substrate Thickness	0.22	±0.02 mm	PCB base substrate thickness

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7. Recommended Schematic

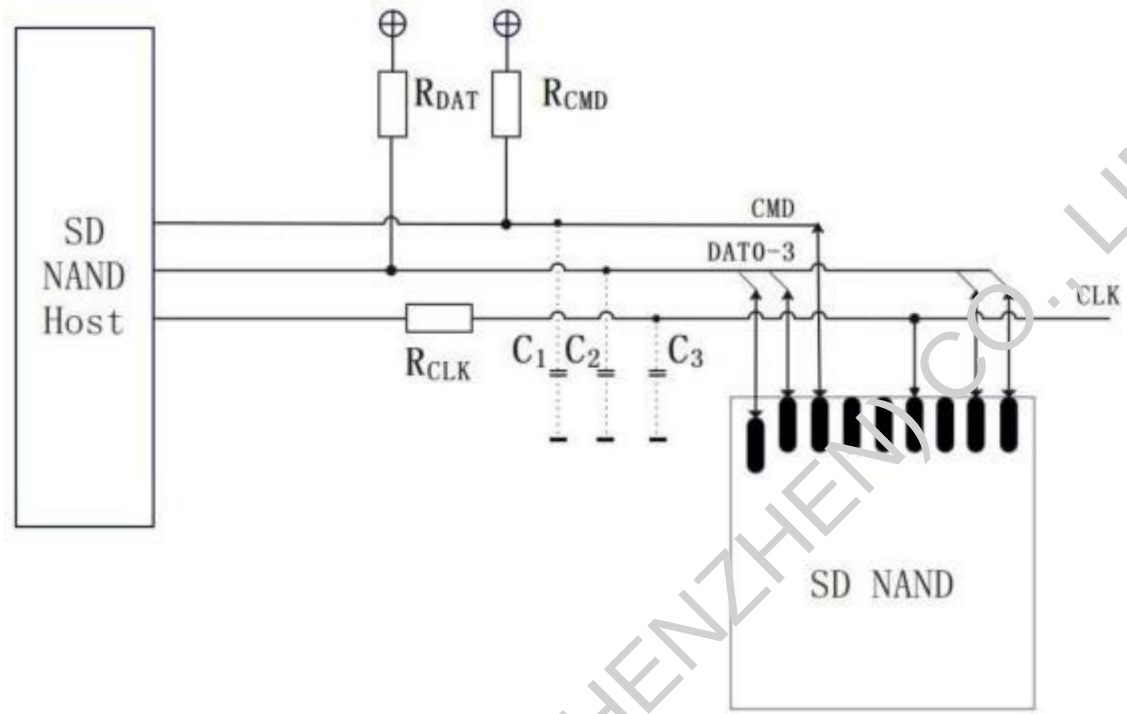


Figure 4: Recommended Schematic

Note: *RDAT and RCMD (10K-100kΩ) are pull-up resistors protecting the CMD and the DAT lines against bus floating when SD NAND is in a high-impedance mode. The host shall pull-up all DAT0-3 lines by RDAT. even if the host uses the SD NAND in 1-bit mode only in SD mode. It is recommended to place a 2.2uF decoupling capacitor on VCC. RCLK reference value 0~120Ω*

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8. Commands

Command Types

There are four kinds of commands defined to control the SD Memory Card:

- Broadcast commands (bc), no response - The broadcast feature is only valid if all the CMD lines are connected together in the host. If they are separated, each card will accept it separately in its turn.
- Broadcast commands with response (bcr) response from all cards simultaneously - Since there is no Open Drain mode in SD Memory Card, this type of command shall be used only if all the CMD lines are separated - each card will accept and respond to the command separately.
- Addressed (point-to-point) commands (ac) no data transfer on DAT
- Addressed (point-to-point) data transfer commands (adtc) data transfer on DAT.

All commands and responses are sent over the CMD line of the SD Memory Card. Command transmission always starts with the left bit of the bit string corresponding to the command codeword.

Command Format

All commands have a fixed code length of 48 bits, requiring a transmission time of 1.92 µs @ 25 MHz and 0.96 µs @ 50 MHz.

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width(bits)	1	1	6	32	7	1
Value	"0"	"1"	x	x	x	"1"
Description	Start bit	Transmission bit	Command index	Argument	CRC7	End bit

Command Classes

The command set of the SD Memory Card system is divided into several classes. Each class supports a set of card functionalities, and determines the setting of CCC based on the card's functionalities, and determines the setting of CCC

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based on the card's supported commands. A CCC bit corresponding to a supported command number is set to 1. A class that includes mandatory commands is always set to 1. Cards with specific functions may need to support some optional commands. For example, Combo Card shall support CMD5.

Class 0, 2, 4, 5 and 8 are mandatory and shall be supported by all SD Memory Cards. Class 7 (Lock Card) is supported by this device. The other classes are optional. The supported Card Command Classes (CCC) are coded as a parameter in the Card Specific Data (CSD) register of each card, providing the host with information on how to access the card.

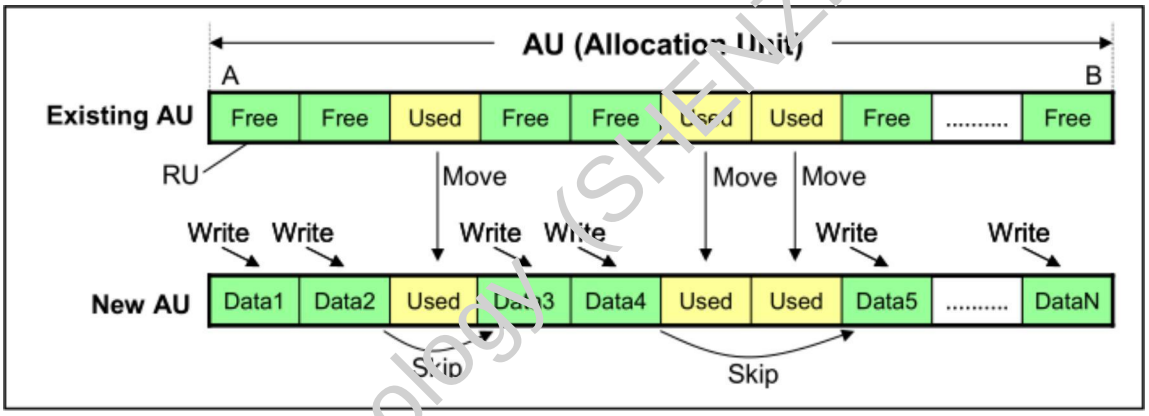
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Card Command Class (CCC)		0	1	2	3	4	5	6	7	8	9	10	11
Supported commands	class description	basic	reserved	block read	reserved	block write	erase	write protection	lock card	application specific	I/O mode	switch	reserved
CMD0	Mandatory	+											
CMD2	Mandatory	+											
CMD3	Mandatory	+											
CMD4	Mandatory	+											
CMD5	Optional										+		
CMD6[2]	Mandatory											+	
CMD7	Mandatory	+											
CMD8[3]	Mandatory	+											
CMD9	Mandatory	+											
CMD10	Mandatory	+											
CMD11[5]	Optional	+											
CMD12	Mandatory	+											
CMD13	Mandatory	+											
CMD15	Mandatory	+											
CMD16	Mandatory			+		+			+				
CMD17	Mandatory			+									
CMD18	Mandatory			+									
CMD19[5]	Optional			+									
CMD20[6]	Optional			+		+							
CMD23[7]	Optional			+		+							
CMD24[1]	Mandatory					+							
CMD25[1]	Mandatory					+							
CMD27[1]	Mandatory					+							
CMD28	Optional							+					
CMD29	Optional							+					
CMD30	Optional							+					
CMD32[1]	Mandatory						+						
CMD33[1]	Mandatory						+						
CMD34-37[2]	Optional											+	
CMD38[1]	Mandatory						+						
CMD40	Optional								+				
CMD42[4]	(Note 4)								+				
CMD50[2]	Optional											+	
CMD52	Optional										+		
CMD53	Optional										+		
CMD55	Mandatory									+			
CMD56	Mandatory									+			
CMD57[2]	Optional											+	
ACMD6	Mandatory									+			
ACMD13	Mandatory									+			
ACMD22[1]	Mandatory									+			
ACMD23[1]	Mandatory									+			
ACMD41[1]	Mandatory									+			
ACMD42	Mandatory									+			
ACMD51	Mandatory									+			

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9. Write Performance

The table below describes the typical data management behaviour when the host writes RUs within an AU. When the host writes to a fragmented AU, the card prepares a new AU by copying the used RUs and writing the new RUs. Location A is at the start of the AU boundary, and location B is at the end of the AU boundary. From A to B, the host shall write data to free RUs contiguously and skip used RUs (shall not skip any free RU). The card may indicate busy status to the host during internal write and data movement operations. The total write time from A to B can be calculated by summing up the write time of free RUs and the moving time of the used RUs. The number of used RUs (Nu) is counted over one AU, and the number of free RUs is expressed as (N RU – Nu).



Example of writing Fragmented AU

Note For this device, the Allocation Unit (AU) size is 128KB, compliant with Class 4 speed grade.

The Performance Write (Pw) is defined as a minimum average write performance over an AU. It is calculated as the average of all sequential RU write operations to one complete, non-fragmented AU.

The Performance Move (Pm) is defined as a minimum average move performance. It is calculated as the average of sequential RU move operations over one complete AU. A move is an internal operation of the card, so SD clock

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frequency does not affect the time of the move operation. In case the card does not have to move RU, Pm should be considered as infinity (1/Pm = 0).

Note that Speed Class 10 shall not use the Pm value stored in the SD Status to calculate performance in any fragmented AU. Class 10 performance is defined only for entirely free AUs.

10. Read Performance

Two types of read performances are defined. Either type of read operation can be inserted during write operations. All read operations, regardless of read address, shall meet this performance specification.

(1) Read Performance of Stream Data
This is simply called **Read Performance (Pr). Pr** is defined as minimum average random RU read performance. The average is measured over 256 random single RU read operations. Each RU is read by a multiple-read command. Pr shall be greater than or equal to Pw.

(2) FAT and Directory Entry Read Time
T_{FR}(4KB) is defined as the maximum time to read a 4KB FAT and Directory Entry. The **FAT and Directory Entry Read Time** (**S_{FR} [KB]**) is defined using the CEIL function:

FAT Read Time of S_{FR} [KB]: $T_{FR}(S_{FR}) = \left\lceil \frac{S_{FR}}{4KB} \right\rceil \cdot T_{FR}(4KB)$ .....(2)

(: CEIL function - Convert decimal fraction x to the smallest integer greater than or equal to x.)

11. SPI Mode

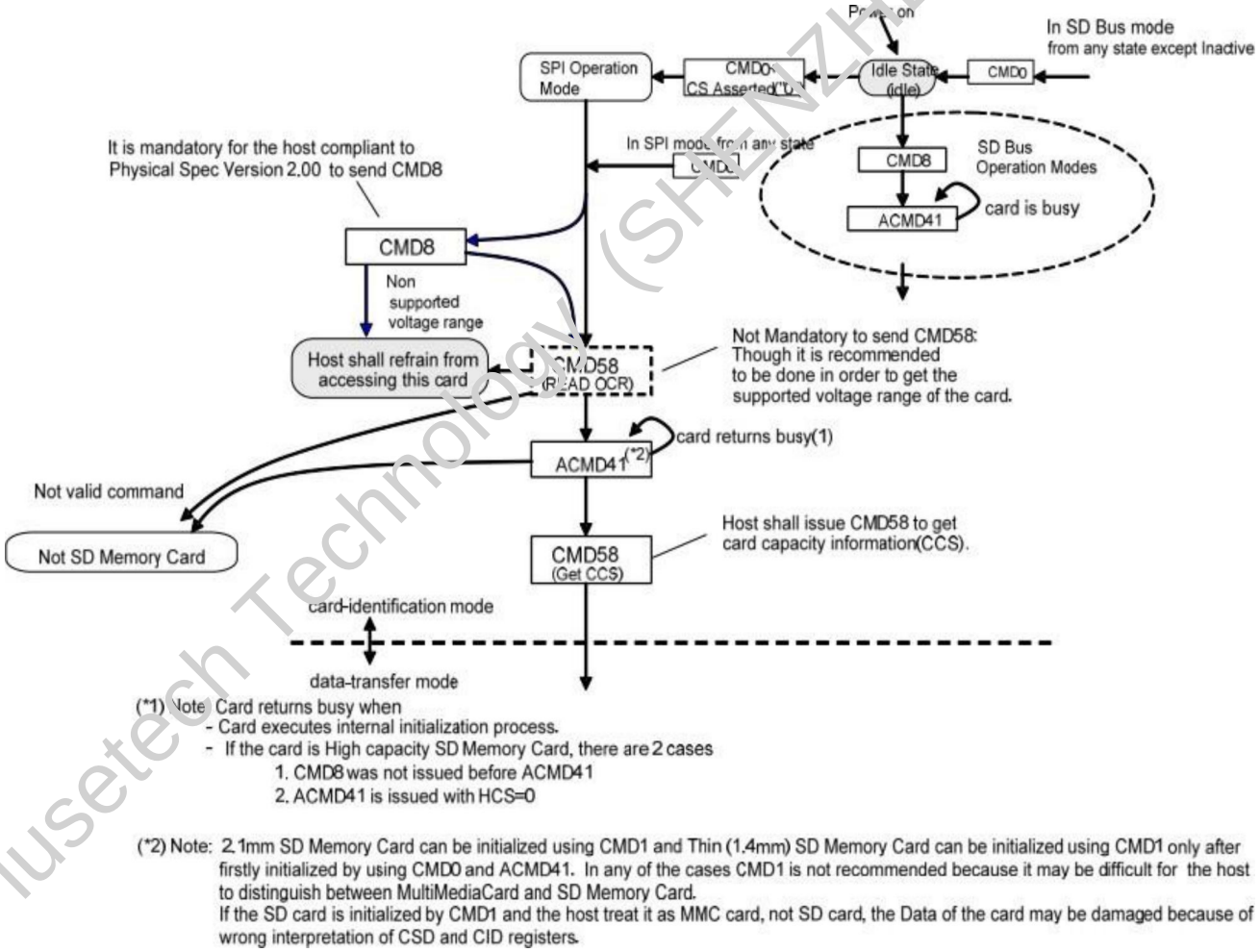
The SPI mode is a secondary communication protocol supported by Flash-based SD Memory Cards. This mode is a subset of the SD Memory Card protocol, designed to communicate with SPI channels commonly found on microcontrollers from various vendors. The interface mode is selected during the first reset command after power-up (CMD0) and cannot be changed once the part is powered on.

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The SPI standard defines only the physical link, not the complete data transfer protocol. The SD Memory Card SPI implementation uses a subset of the SD Memory Card protocol and command set.

The advantage of SPI mode is the ability to use off-the-shelf host controllers, minimizing design-in effort. The disadvantage is lower performance compared to SD mode (e.g., single data line and per-card hardware CS signal)..

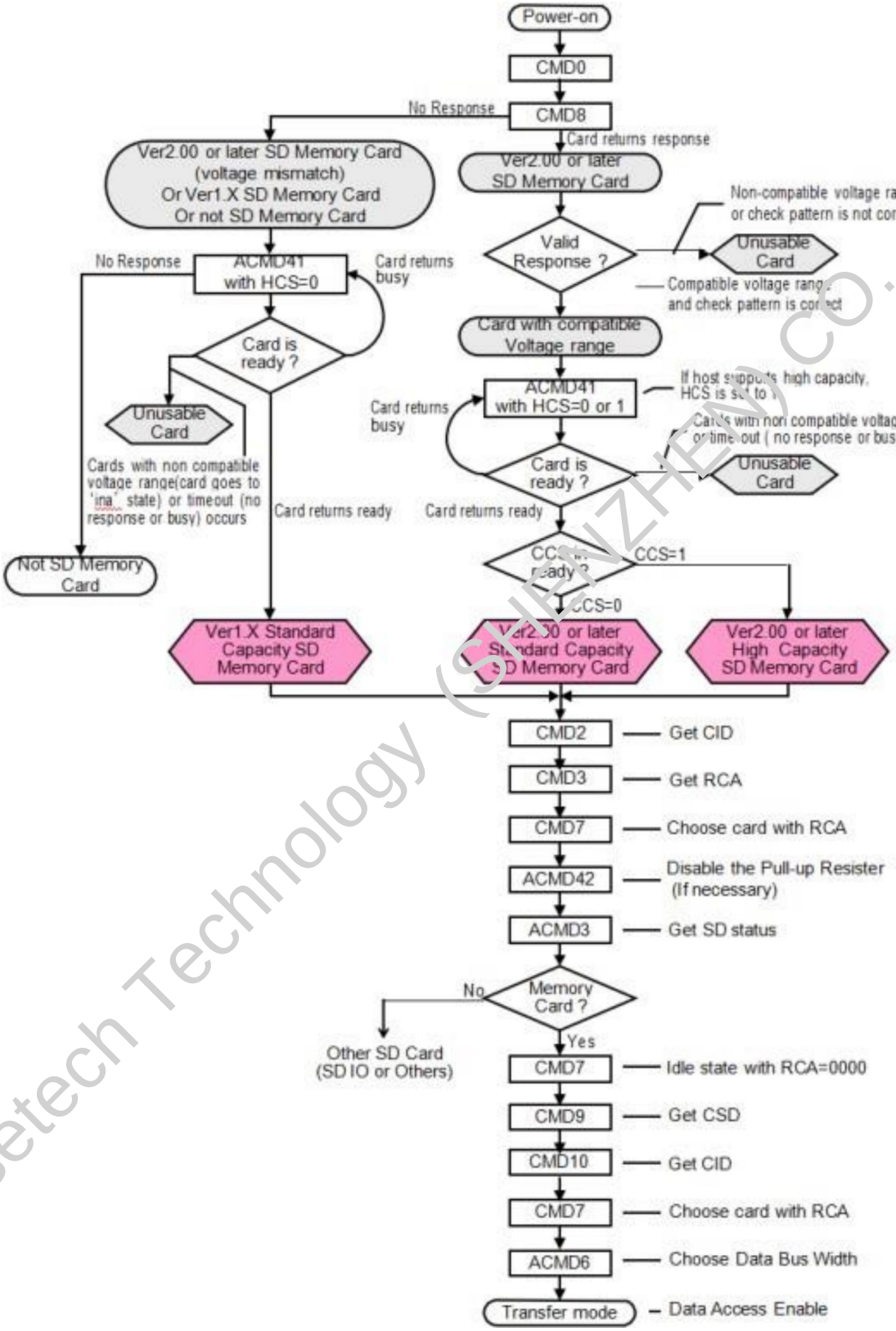
Commands and functions defined after SD Specification Version 2.00 in SD mode are not supported in SPI mode. The card may respond to such commands even in SPI mode, but the host shall not use them.



card state Diagram (SPI mode)

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12. SD Mode

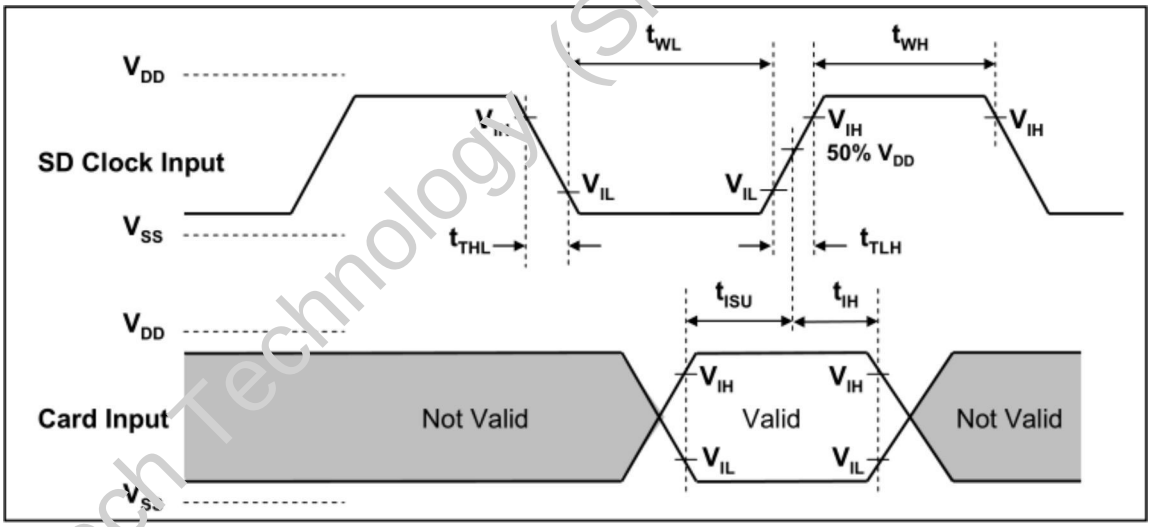


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13. DC Characteristics

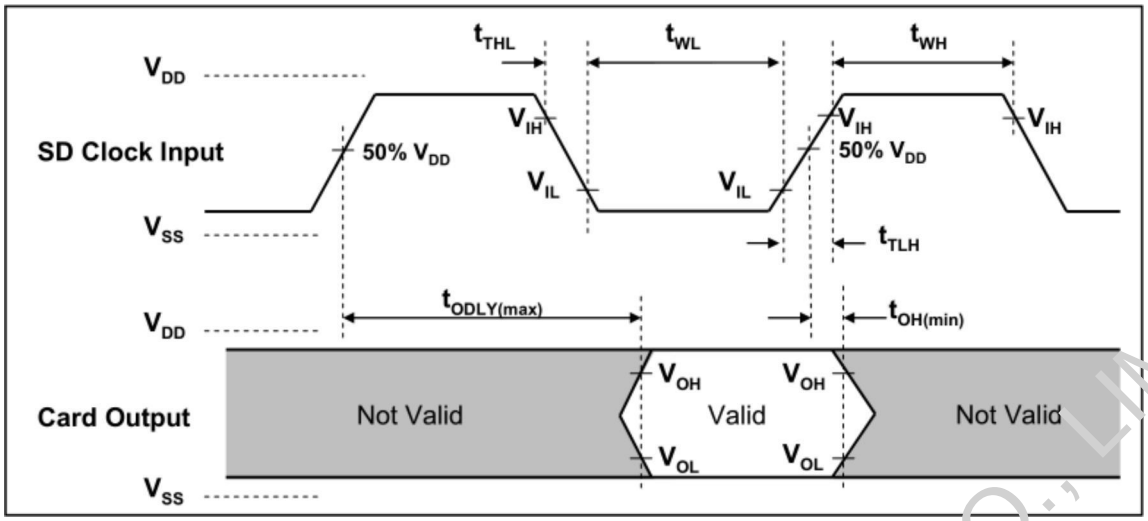
Symbol	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input low voltage		VSS-0.3		0.25VCC	V
V_{IH}	Input high voltage		0.625VCC		VCC+0.3	V
V_{OL}	Output low voltage	IOL=100μA @VCC_min			0.125VCC	V
V_{OH}	Output high voltage	IOH=100μA @VCC_min	0.75VCC			V
I_{IN}	Input leakage current	VIN=VCC or 0	-10	+/-1	10	μA
I_{OUT}	Tri-state output leakage current		-10	+/-1	10	μA
I_{STBY}	Standby current	3.3V@clock stop		150	200	μA
I_{OP}	Operation current	3.3v@50MHz (Write)		15	25	mA
		3.3v@50MHz (Read)		15	25	mA

14. Bus Timing (High-Speed Mode)



card Input Timing (High speed card)

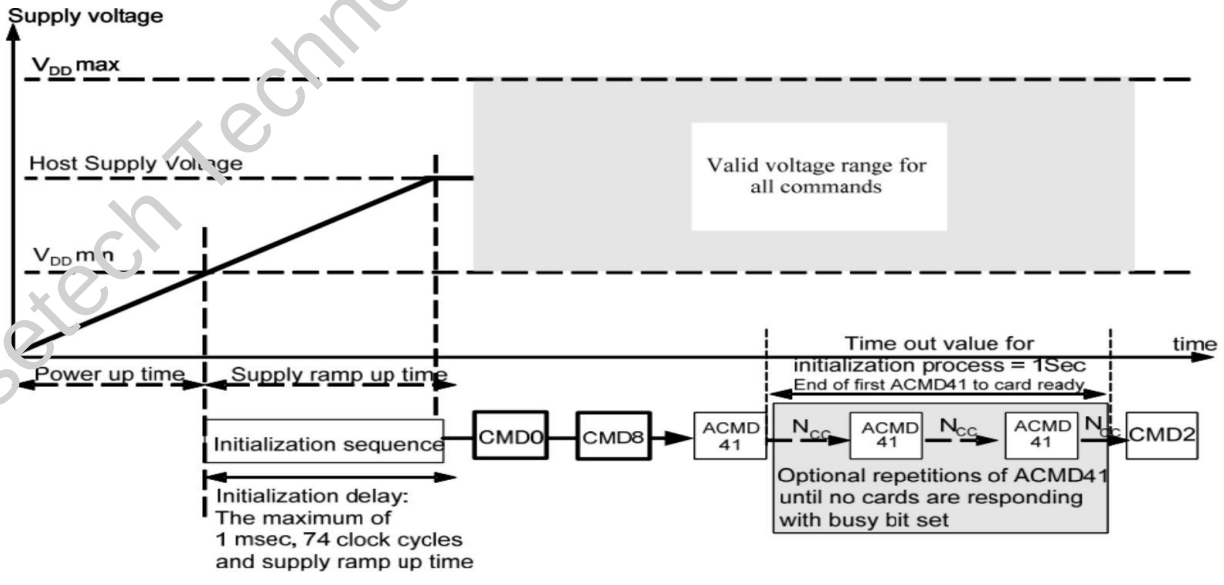
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card output Timing(High speed Mode)

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}),					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{CARD} ≤ 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{CARD} ≤ 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{CARD} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{CARD} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{CARD} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{CARD} ≤ 10 pF (1 card)

15. Power Up



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Power-up Diagram

'Power up time' is defined as voltage rising time from 0 volt to VDD min (refer to DC Characteristics) and depends on application parameters such as the maximum number of SD Cards, bus length and power supply characteristics.

'Supply ramp up time' is the time required for the supply voltage to reach the stable operating level, and the waiting time before the SD card can accept the first command.

The host shall supply power to the card such that VDD reaches VDD min within 250ms, and provide at least 74 SD clock cycles while keeping the CMD line high. In SPI mode, CS shall be held high during the 74 clock cycles.

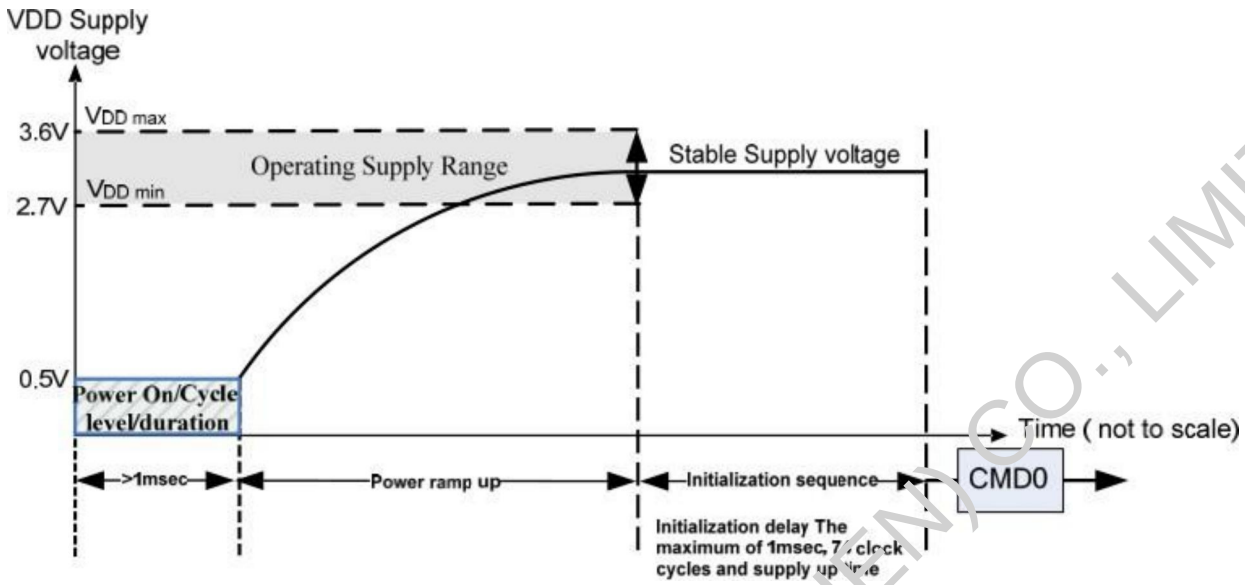
After power up (including hot insertion, i.e. inserting a card when the bus is operating) the SD Card enters the idle state. In case of SD host, CMD0 is not necessary. In case of SPI host, CMD0 shall be the first command to send the card to SPI mode.

CMD8 is newly added in the Physical Layer Specification Version 2.00 to support multiple voltage ranges and used to check whether the card supports supplied voltage. The version 2.00 or later host shall issue CMD8 and verify voltage before card initialization. The host that does not support CMD8 shall supply high voltage range.

ACMD41 is a synchronization command used to negotiate the operation voltage range and to poll the cards until they are out of their power-up seauence, In case the host system connects multiple cards the host shall check that all cards satisfy the supplied voltage. Otherwise, the host should select one of the cards and initialize.

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Power Up Time



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